DEPARTMENT OF TRANSPORTATION
FEDERAL AVIATION ADMINISTRATION

INTERFACE CONTROL DOCUMENT

MULTIMODE DIGITAL RADIO/RADIO INTERFACE UNIT

The NEXCOM Integrated Product Team, AND-360

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RECORD OF CHANGES

Revision	Date	Action
0.0	7/5/2000	Version 1.2a MDR/RIU ICD Draft Baselined as Revision 0.0 IRB CR 0089
1.0	8/8/2000	Incorporation of the following approved IRB CRs: IRB CR 0097 IRB CR 0124 IRB CR 0125 IRB CR 0126 IRB CR 0127 IRB CR 0128 IRB CR 0129 IRB CR 0130 IRB CR 0131 IRB CR 0132 IRB CR 0133 IRB CR 0134 IRB CR 0135 IRB CR 0136 IRB CR 0137 IRB CR 0138 IRB CR 0139 IRB CR 0140 IRB CR 0141 IRB CR 0142 IRB CR 0143 IRB CR 0170
2.0	9/20/2000	Incorporation of the following approved IRB CRs: IRB CR 0197 IRB CR 0198 IRB CR 0199 IRB CR 0232

		IRB CR 0233 IRB CR 0234 IRB CR 0235 IRB CR 0236 IRB CR 0238 IRB CR 0239 IRB CR 0240 IRB CR 0245 IRB CR 0249 IRB CR 0253 IRB CR 0269 IRB CR 0270
3.0	7/23/2001	Incorporation of the following approved IRB CRs: IRB CR 0275 IRB CR 0278

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1.0 SCOPE

1.1 Scope

This Interface Control Document (ICD) describes the design characteristics for the interfaces between the Very High Frequency (VHF) Multimode Digital Radio (MDR) and the Radio Interface Unit (RIU). This ICD satisfies the design requirements contained in the following document:

- FAA-E-2938, Subsystem Specification for the Multimode Digital Radio Supporting Programmable VHF Multimode Communication Equipment Operating within the Frequency Range of 112.000 – 137.000 MHz, Version 3.0, September 20, 2000.

1.2 Subsystem Responsibility List

Table 1-1 identifies the subsystems and the responsible Federal Aviation Administration (FAA) Office.

Table 1-1. Subsystem Responsibility List

Subsystem	Common Name	FAA-Office
MDR	Multimode Digital Radio	AND-360
RIU	Radio Interface Unit	AND-360

1.3 Document Organization

This document is written in accordance with FAA-STD-025d and organized as follows:

- Section 1, SCOPE, identifies the interfacing systems and provides a summary of the contents of this document.
- Section 2, APPLICABLE DOCUMENTS, provides a list of referenced documents, including both Government and Non-government documents.
- Section 3, INTERFACE DESIGN CHARACTERISTICS, provides the general, functional, and physical information about the interface.
- Section 4, QUALITY ASSURANCE PROVISIONS, provides a description of the verification process for the requirements presented in Section 3.
- Section 5, PREPARATION FOR DELIVERY, specifies any special preparation requirements for delivery.
- Section 6, NOTES, provides a list of applicable definitions used in this document.

2.0 APPLICABLE DOCUMENTS

The following documents form a part of this document to the extent specified herein. The following references are the documents used, by date, in this standard.

2.1 Government Documents

STANDARDS:

FAA-STD-025d	Preparation of Interface Documentation Standards, October 1995
FAA-STD-057	Airport Fiber Optic Communication System Standards, DRAFT
47 CFR	Code of Federal Regulations, Title 47, FCC Rules and Regulations, Part 68, Revised 1 October 1998

DOCUMENTS:

FAA-E-2938	Subsystem Specification for the Multimode Digital Radio Supporting Programmable Very High Frequency (VHF) Multimode Communication Equipment Operating within the Frequency Range of 112.000-137 MHz, Version 3.0, September 20, 2000.
FAA-E-2944	Multimode Digital Radio (MDR) Maintenance Data Terminal (MDT) Maintenance Application Software Requirements Specification, Version 0.0, September 20, 2000.

2.2 Non-Government Documents

ANSI:

ANSI T1.403	American National Standard for Telecommunications - Carrier-to-Customer Installation - DS1 Metallic Interface, 1995

ICAO:

VHF Digital Link (VDL) TDMA Mode (Mode 3) Standards and Recommended Practices (SARPS) Annex 10, Volume III, Part 1, Chapter 6

ISO/IEC:

ISO/IEC 3309	Information Technology – Telecommunications and Information Exchange Between Systems – High-level Data Link Control (HDLC) Procedures – Frame Structure, 1993
ISO/IEC 4335	Information Technology – Telecommunications and Information Exchange Between Systems – High-level Data Link Control (HDLC) Procedures – Elements of Procedures, 1993

ISO/IEC 7498	Information Technology – Open Systems Interconnection – Basic Reference Model, November 1994
ISO/IEC 7809	Information Technology - Telecommunications and Information Exchange Between Systems - High-level Data Link Control (HDLC) Procedures - Classes of Procedures, 1993

ITU-T:

ITU-T G.824-1993	Digital Networks-The Control of Jitter and Wander within Digital Networks which are Based on the 1544 kbit/s Hierarchy, March 1993

RTCA:

RTCA DO-224a	Signal in Space Minimum Aviation System Performance Standards (MASPS) for Advanced VHF Digital Data Communications Including Capability with Digital Voice Technique

2.3 Document Sources

2.3.1 FAA Documents

Copies of FAA specifications, standards, and publications may be obtained from the Contracting Officer, Federal Aviation Administration, 800 Independence Avenue, S.W., Washington, D.C. 20591. Requests should clearly identify the desired material by number and date, and state the intended use of the material.

2.3.2 Military and Federal Documents

Single copies of unclassified military and federal specifications, standards, and publications may be obtained by writing the Naval Publications and Forms Center, 5801 Tabor Avenue, Philadelphia, PA, 19120; or by calling (215) 697-3321 Monday through Friday, 8:00 a.m. to 4:30 p.m. Eastern Standard Time (EST).

2.3.3 American National Standards Institute and International Organization of Standardization Documents

Copies of American National Standards Institute (ANSI) and International Organization of Standardization (ISO) documents may be obtained from the American National Standards Institute, 11 West 42nd Street, New York, NY, 10036, or through the web site http://www.ansi.org.

2.3.4 International Civil Aviation Organization Documents

Copies of final products of International Civil Aviation Organization (ICAO) documents may be obtained from the ICAO Library is 999 University Street, Montreal, Quebec H3C 5H7, Canada, or through the web site http://www.icao.org.

2.3.5 International Telecommunications Union Telecommunication Standardization Sector Documents

Copies of International Telecommunications Union Telecommunication Standardization Sector (ITU-T) documents may be obtained from the ITU, Place des Nations, CH-1211 Geneva 20, Switzerland, through the web site http://www.itu.int.

2.3.6 RTCA Documents

Copies of RTCA documents may be obtained from the RTCA Inc., 1140 Connecticut Avenue, N.W., Suite 1020, Washington, DC 20036-4001 or by calling (202) 833-9339, or through the web site http://www.rtca.org.

3.0 INTERFACE DESIGN CHARACTERISTICS

This section specifies the general, functional, and physical design characteristics of the MDR/RIU interface.

3.1 General Design Characteristics

The general design characteristics are based on the subsystem definitions, the interface design considerations, and planned operational configurations.

3.1.1 Subsystem Definition

The MDR subsystem is implemented as two units, a separate VHF radio transmitter and a separate VHF radio receiver, which are not necessarily collocated. An MDR transmitter and MDR receiver pair provides the majority of the physical layer functionality described in the VDL Mode 3 MASPS in RTCA DO-224a. This functionality is summarized as follows:

- Synchronization Sequence Generation and Detection
- Gray Code Encoding and Decoding
- Differential Encoding and Decoding
- Bit Scrambling and Descrambling
- Golay Forward Error Correction (FEC)
- Modulation and Demodulation

In Segment 1 Step 1, MDR transmitters and MDR receivers will operate in 25 kHz double sideband (DSB)-Amplitude Modulation (AM) analog mode. This mode of operation is needed to support current Air Traffic Control (ATC) voice operations. In Segment 1 Step 2, MDR transmitter and MDR receivers will operate in VDL Mode 3 for digital voice communications. VDL Mode 3 uses Time Division Multiple Access (TDMA) techniques enabling multiple users to share the same frequency for the exchange of both voice and data information. MDR transmitter and MDR receiver functionality is defined in FAA-E-2938.

In Segment 1 Step 1, legacy Radio Control Equipment (RCE) will provide the currently used analog interface and control functions to MDR transmitters and receivers, which will operate in 25 kHz DSB-AM analog mode to maintain the current voice communications environment. In Segment 1 Step 2, the RIU will provide the functionality needed to allow MDR transmitters and MDR receivers to operate in VDL Mode 3 for digital voice communications only. In Segment 2, the addition of VDL Mode 3 data communications will require a Ground Network Interface (GNI) subsystem at the control site to provide data to the RIU. The functions provided by the RIU are summarized as follows:

- Reed-Solomon (R-S) FEC
- Media Access Control (MAC)
- Burst Formatting
- Link Management (radio level)

- Data Link Service

3.1.2 Interface Design Considerations

The interface between the MDR and the RIU carries a number of distinct types of information:

- VDL Mode 3 payload data (Management-, Voice-, and Data-Bursts)
- Radio control and status (e.g., current operating frequency, audio output level, , power output (AM))
- Pulse Coded Modulated (PCM) voice (to/from radio when operating in DSB-AM mode)
- System timing information (needed in VDL Mode 3 for accurate synchronization of the transmitter, and to determine the receiver squelch window)

The properties of the four data types identified above are entirely different. The following observations apply:

- VDL Mode 3 has a basic RF channel rate of 31.5 kbit/s and some strict real-time requirements.
- The VDL Mode 3, radio control and status have relaxed timing requirements. Although covering a large variety of commands and responses, the frequency of occurrence and the average data rates are low.
- System timing information has strict real-time requirements, but the amount of information transferred is small.
- The16-bit linear PCM voice data rate is 128 kbit/s, and has real-time requirements. The PCM voice interface will only operate in the DSB-AM mode.

In addition to the various types of data supported across the interface, the interface design characteristics are affected by the nature of the relative locations of the RIU and the MDR when deployed in the field. On one extreme, the RIU and the MDR equipment would be co-located at the Radio Control Facilities (RCF) (often the case in the en-route communication facilities). On the other extreme, distances of up to 4 miles (often the case in the terminal communication facilities) can separate the RIU from the MDR receiver.

3.1.3 Operational Configurations

Figures 3-1 and 3-2 depict the configurations supported by the interface defined in this ICD. The MDR to RIU interface consists of a number of standard fractional T1 ports. Figure 3-1, illustrates a typical remote site, with co-located transmitters and receivers, (Main and Standby NEXCOM transmitters and receivers). Figure 3-2 illustrates a split remote site, with the transmitters and receivers installed at two separate locations.

Where required (typically in airport environments using separated transmit and receive sites), the T1 ports in the RIU and remote transmitter and receivers will be directly connected to a long-haul multi-port fiber optic multiplexer/demultiplexer (Fiber Mux) that is expected to be available at the site. Procurement and deployment of the Fiber Muxes are not a part of NEXCOM, but under a separate FAA Program Office.

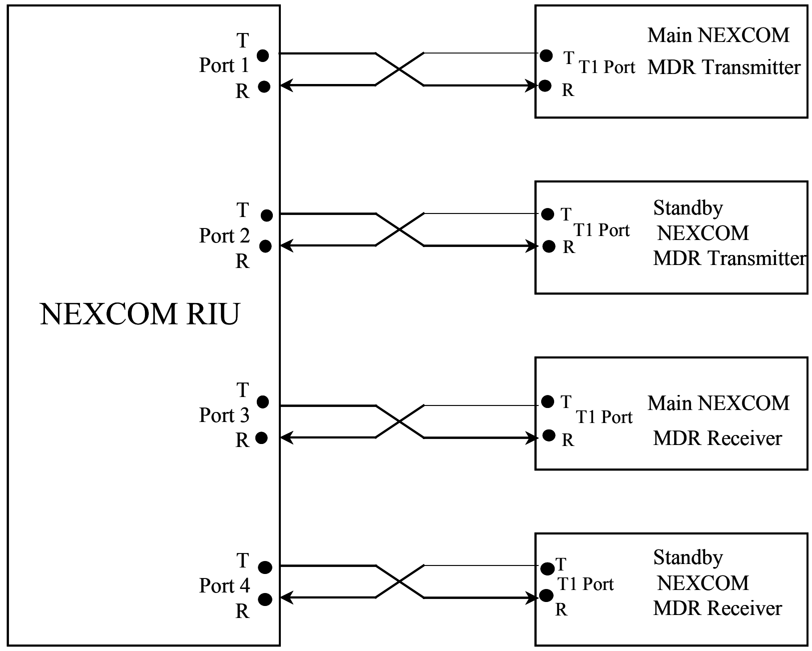


Figure 3-1. Co-located Transmitter and Receiver

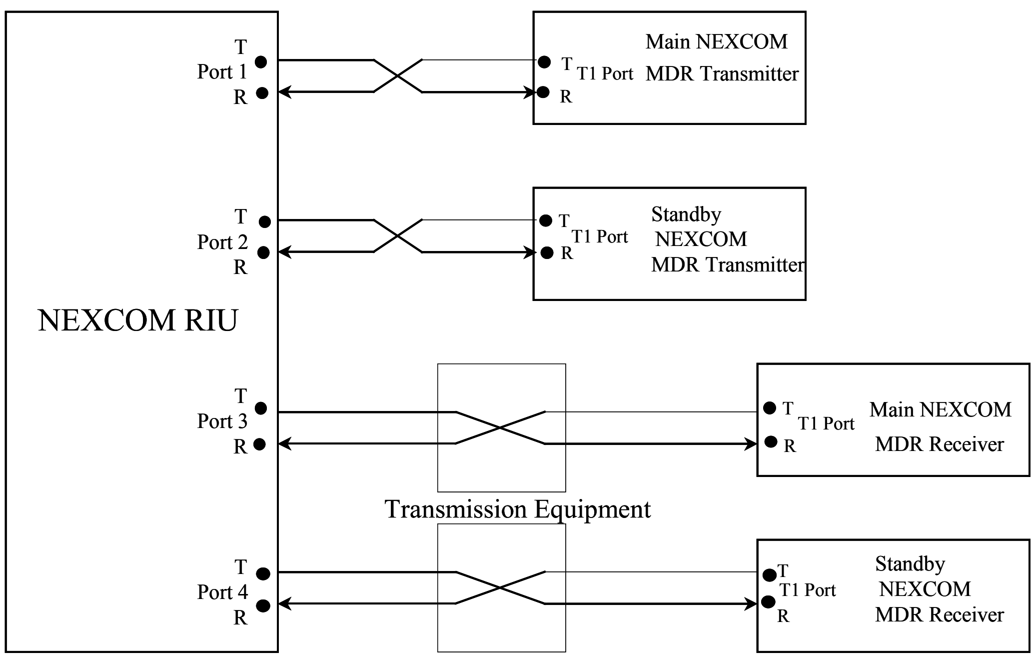


Figure 3-2. Transmitter and Receiver at Separate Locations

3.1.4 Interface Boundary Points

All requirements imposed by this document on either the RIU or the MDR are applicable to and measured at the interface boundaries. The interface boundary for the RIU is the T1 connector on the RIU. The interface boundary for the MDR is the T1 connector on the MDR.

3.2 Functional Design Characteristics

The MDR/RIU Interface is organized according to the ISO/IEC 7498, Information Technology – Open Systems Interconnection – Basic Reference Model. The design for this interface utilizes three of the seven OSI-type interface layers, the Application Layer (level 7), Data Link Layer (level 2) and Physical Layer (level 1). Although referenced in this document, levels 3 through 6 are not applicable.

3.2.1 Application Processes

3.2.2 OSI-type Data Interface

3.2.2.1 Application Layer

3.2.2.1.1 Voice Services

3.2.2.1.1.1 Digital Transmission

The RIU will send an integral number of vocoder frames within each RIU/MDR packet up to a total of 6 frames.

3.2.2.1.1.2 AM Transmission

The RIU will send linear PCM voice to the transmitter and receive linear PCM voice from the receiver during DSB-AM modes of operation. The PCM voice will be encoded using an 8 kHz sampling rate at a resolution of 16 bits per sample.

3.2.2.1.2 Data Services

The RIU will send Reed-Solomon (72, 62) code words to the MDR transmitter and receive them from the MDR receiver.

3.2.2.1.3 VDL Mode 3 Management Services

The RIU will send unprotected (Non-Golay) management bursts to the MDR transmitter and receive them from the MDR receiver.

3.2.2.1.4 Remote Maintenance Monitoring and Control (RMMC) Services

The MDR-RIU interfaces will carry RMMC information to and from the MDR receivers and transmitters. MDR monitoring and control messages will be exchanged between the MDR and the RIU to support remote monitoring and control of the MDR.

3.2.2.1.4.1 Control Messages

As specified in FAA-E-2938, the MDR will receive control messages from the RIU. All control messages will be explicitly acknowledged with a control reply message indicating the acceptance or non-compliance of the request. Non-compliance is defined as the MDR not adjusting the parameter as requested. The MDR will indicate the current value of the parameter after rejection in the reply indicating non-compliance.

3.2.2.1.4.2 Monitoring Messages

As specified in FAA-E-2938, the MDR will transmit monitoring messages to the RIU in response to a request, and upon Alert and Alarm threshold crossings.

3.2.2.1.4.3 MDR RMMC Parameters

3.2.2.1.4.3.1 MDR Control Parameters

a) The MDR will support the control parameters identified in Table 3-1. The attributes of the control parameters are defined in FAA-E-2938.
b) The bit formats of the control packets (Refer to section 3.2.2.6.5.1.6) are defined in sections 3.2.2.1.4.3.1.1 through 3.2.2.1.4.3.1.35. The ID number in Table 3-1 corresponds to the Control Type (CTYPE) field defined in the general message structure format.
c) The Protocol Identifier (PID) field (as defined in section 3.2.2.6.5.1.6) is set to all zeros to use the following bit formats. For each octet, bit 1 is the least significant bit (lsb) and bit 8 is the most significant bit (msb). Lower numbered octets contain higher order bits for fields that cross octet boundaries. Reserved fields are all zeroes.

Table 3-1. Control and Monitor Parameters

Control Parameters		Monitor Parameters	
ID	**Name**	**ID**	**Name**
1	Log-In/Log-Out	1	Event Log
2	Current Frequency	2	Current Frequency
3	Lowest Tunable Frequency	3	Lowest Tunable Frequency
4	Mode of Operation	4	Mode of Operation
5	MDR State	5	MDR State
6	Threshold Setting	6	Threshold Setting
7	Time	7	Time
8	Squelch RF Threshold Level Setting (AM)	8	Squelch RF Threshold Level Setting (AM)

Table 3-1. Control and Monitor Parameters (continued)

Control Parameters		Monitor Parameters	
ID	**Name**	**ID**	**Name**
9	Squelch Audio Signal-to-Noise Level Setting (AM)	9	Squelch Audio Signal-to-Noise Level Setting (AM)
10	Audio Output Level (AM)	10	Audio Output Level (AM)
11	Receiver Mute (AM)	11	Receiver Mute (AM)
12	Power Output (AM)	12	Power Output Setting (AM)
13	Transmitter Modulation % (AM)	13	Transmitter Modulation % Setting (AM)
14	ATR Switch State	14	ATR Switch State
15	Switch Software Version	15	Software Version
16	N1 (Number of Information Bits)	16	N1 (Number of Information Bits)
17	T1 (Link Response Timer)	17	T1 (Link Response Timer)
18	T3 (Reassembly Timer)	18	T3 (Reassembly Timer)
19	HDLC Channel Number	19	HDLC Channel Number
20	Transmission Timeout (AM)	20	Transmission Timeout Setting (AM)
21	Squelch Enable/Disable (AM)	21	Squelch Enable/Disable (AM)
22	ATR Switch Mode	22	ATR Switch Mode
30	Request Read Back	30	Reserved
31	Audio Input level (AM)	31	Audio Input Level Setting
32	Reserved	32	Reserved
33	Reserved	33	Reserved
34	MAC Timing Offset Correction (VDL Mode 3)	34	MAC Timing Offset Correction (VDL Mode 3)
35	Suppress Alert/Alarm	35	Suppress Alert/Alarm Setting
36	Reset	36	Reserved
37	Software Upload Enable/Disable	37	Software Upload Setting
38	Software Upload	38	Reserved
39	Receiver Mute Level (AM)	39	Receiver Mute Level Setting
40	Test PTT (AM)	40	PTT Setting
41	Public Key Maintenance	41	Public Key List
42	T2 (Link Retransmission Timer)	42	T2 (Link Retransmission Timer)
50	Reserved	50	MDR ID Number
51	Reserved	51	RF Input Power Level (AM)
52	Reserved	52	Squelch Break Status (AM)

Table 3-1. Control and Monitor Parameters (continued)

Control Parameters		Monitor Parameters	
ID	**Name**	**ID**	**Name**
53	Reserved	53	In-Service Time
54	Reserved	54	RIU Timing Offset Change (VDL Mode 3)
55	Reserved	55	Transmit Antenna VSWR
56	Reserved	56	Reserved
57	Reserved	57	Measured Power Output
58	Reserved	58	Measured Transmitter Modulation %

3.2.2.1.4.3.1.1 Log-In/Log-Out (ID 1)

a) The bit format of the Log-In/Log-Out parameter **shall**[81] be encoded/decoded as indicated in Figure 3-3.

	First bit Trans- mitted	Bit Number						
Octet	1	2	3	4	5	6	7	8
1	Month				0	0	0	0
2	Day					0	0	0
3	Year-2000							
4	Hours					0	0	0
5	Minutes						0	0
6	User ID							
...								
25								
26	Terminal ID							
...								
65								
66	Security Token							
...								
X*								

- Month, Day, Year, Hours and Minutes fields are encoded as specified in 3.2.2.1.4.3.1.7.
- User ID field consists of 20 ASCII characters, zero padded.
- Terminal ID field consists of 40 ASCII characters.
- The Log-In message is sent complete, while the Log-Out message terminates with Terminal ID (Octet 65).
- X*: Size of Security Token is implementation specific.
- The security token is comprised of:
    - Octets 66 to 105: FAA data field (40 ASCII characters)
    - Octets 106 to X: Digital Signature (and associated data if required).

Figure 3-3. Log-In/Log-Out Parameter Format

3.2.2.1.4.3.1.2 Current Frequency (ID 2)

a) The bit format of the Current Frequency parameter **shall**[83] be encoded/decoded as indicated in Figure 3-4.

	First bit Trans-mitted	Bit Number						
Octet	1	2	3	4	5	6	7	8
1				FrequencyID				(msb)
2	(lsb)							

- FrequencyID is encoded as INT((F*1000-112000) / 8.333) where F is the desired frequency in MHz, expressed with eight significant digits (e.g. 132.00833).
- The INT(x) function yields the integer value of x.
- The frequency begins at 112 MHz and increases in steps of 8 1/3 kHz
- The FrequencyID represents how many 8 1/3 kHz steps above 112 MHz the Frequency is.
- Frequency ID has a valid range of 0 to 2997 in increments of 1.
- The following example illustrates the Frequency and FrequencyID mapping:

Valid FrequencyID for Current Frequency	Frequency
0	112.00000
1	112.00833
2	112.01667
3	112.02500
4	112.03333
5	112.04167
6	112.05000
7	112.05833
8	112.06667
9	112.07500
10	112.08333
11	112.09167
12	112.10000
....	...

Figure 3-4. Current Frequency Parameter Format

3.2.2.1.4.3.1.3 Lowest Tunable Frequency (ID 3)

a) The bit format of the Lowest Tunable Frequency parameter **shall**[87] be encoded/decoded as indicated in Figure 3-5.

	First bit Trans-mitted	Bit Number						
Octet	1	2	3	4	5	6	7	8
1	LT_FrequencyID							(msb)
2	(lsb)							

- LT_FrequencyID is encoded as INT((F*1000-112000) / 8.333) where F is the desired frequency in MHz, expressed with eight significant digits (e.g. 112.02500).
- The INT(x) function yields the integer value of x.
- For the Lowest Tunable Frequency parameter, the frequency F begins at 112 MHz and increases in steps of 25 kHz.
- LT_FrequencyID has a valid range of 0 to 2997 in increments of 3.
- The following example illustrates the Frequency and LT_FrequencyID mapping:

Valid LT_FrequencyID for Lowest Tunable Frequency	Frequency
0	112.00000
3	112.02500
6	112.05000
9	112.07500
12	112.10000
....	...

Figure 3-5. Lowest Tunable Frequency Parameter Format

3.2.2.1.4.3.1.4 Mode of Operation (ID 4)

a) The bit format of the Mode of Operation parameter **shall**[89] be encoded/decoded as indicated in Figure 3-6.

	First bit Trans-mitted	Bit Number						
Octet	1	2	3	4	5	6	7	8
1	MODE							

- Where MODE is encoded as follows:
  0 = 25 kHz DSB-AM
  85 = 8 1/3 kHz DSB-AM
  255 = VDL Mode 3

Figure 3-6. Mode of Operation Parameter Format

3.2.2.1.4.3.1.5 MDR State (ID 5)

a) The bit format of the MDR State parameter **shall**[91] be encoded/decoded as indicated in Figure 3-7.

	First bit Trans-mitted	Bit Number						
Octet	1	2	3	4	5	6	7	8
1	STATE			Reserved				

- Where STATE is encoded as follows:
  0 = OFFLINE
  1 = POWER DOWN (if exercised)
  2 = Reserved
  3 = ONLINE
  4-7 = Reserved

Figure 3-7. MDR State Parameter Format

3.2.2.1.4.3.1.6 Threshold Setting (ID 6)

a) The bit format of the Threshold Setting parameter **shall**[93] be encoded/decoded as indicated in Figure 3-8a.

	First bit Trans-mitted	Bit Number						
Octet	1	2	3	4	5	6	7	8
1	(lsb)			Monitor ID				(msb)
2				Low Alert Threshold				(msb)
3	(lsb)							
4				High Alert Threshold				(msb)
5	(lsb)							
6				Low Alarm Threshold				(msb)
7	(lsb)							
8				High Alarm Threshold				(msb)
9	(lsb)							

- Monitor ID field indicates the particular monitoring ID of which alert and alarm thresholds are changed.
- Alert and Alarm Thresholds are encoded/decoded according to the following:
  - RF Input Power Level, per Figure 3-8b,
  - Measured Power Output, per Figure 3-8c,
  - Measured Transmitter Modulation %, per 3-8d.
- If a particular monitoring parameter requires only one octet, then the second octet of each Alert/Alarm Thresholds (Octets 3, 5, 7 and 9) is set to zero.
- If a particular monitoring parameter has only one threshold, then the other threshold values are set to zero.

Figure 3-8a. Threshold Setting Parameter Format

	First bit Trans-mitted	Bit Number						
Octet	1	2	3	4	5	6	7	8
1	Monitor ID = 51							
2	0	0	0	0	0	0	0	0
3	0	0	0	0	0	0	0	0
4	RF Input Power (for High Alert)							
5	0	0	0	0	0	0	0	0
6	0	0	0	0	0	0	0	0
7	0	0	0	0	0	0	0	0
8	RF Input Power (for High Alarm)							
9	0	0	0	0	0	0	0	0

- RF Input Power field is encoded as:
  Measured RF Input Power Level (dBm) + 110.
- Since the Measured RF Input Power Level has a range of -110 to +15 dBm, the RF Input Power field has a valid range of 0 to 125.

Figure 3-8b. Threshold Setting for Measured RF Input Power Level Format

	First bit Trans-mitted	Bit Number						
Octet	1	2	3	4	5	6	7	8
1	Monitor ID = 57							
2	0	0	0	0	0	0	0	0
3	0	0	0	0	0	0	0	0
4	0	0	0	0	0	0	0	0
5	0	0	0	0	0	0	0	0
6	Measure Power Output Underrun (for Low Alarm)				0	0	0	0
7	0	0	0	0	0	0	0	0
8	Measure Power Output Overrun (for High Alarm)				0	0	0	0
9	0	0	0	0	0	0	0	0

- Measured Power Output Underrun and Measured Power Output Overrun fields are encoded as desired threshold in dB*2, dB, where the desired threshold range is 0.5 to 7 dB, in 0.5 dB steps, and the valid range of Measured Power Output Underrun or Overrun is 0 to 14.
- A Measured Power Output Underrun or Measured Power Output Overrun setting of zero disables the respective Measured Power Output alarm.
- The Measured Power Output alarm setting indicates how many dB under (Underrun) or over (Overrun) the Power Output Setting (ID #12) is the threshold for setting an alarm. For example, with a Power Output set to 39 dBm, a Measured Power Output Underrun of 3 dB and a Measured Power Output Overrun of 5 dB, an alarm would be set if the Measured Power Output falls below 36 dBm, or if the Measured Power Output reaches above 44 dBm.

Figure 3-8c. Threshold Setting for Measured Power Output Format

	First bit Trans- mitted	Bit Number						
Octet	1	2	3	4	5	6	7	8
1	Monitor ID = 58							
2	0	0	0	0	0	0	0	0
3	0	0	0	0	0	0	0	0
4	0	0	0	0	0	0	0	0
5	0	0	0	0	0	0	0	0
6	0	0	0	0	0	0	0	0
7	0	0	0	0	0	0	0	0
8	Measured Transmitter Modulation % (for High Alarm)							
9	0	0	0	0	0	0	0	0

- Measured Transmitter Modulation % is encoded as 0 - 100 in steps of 1.

Figure 3-8d. Threshold Setting for Measured Transmission Modulation %

3.2.2.1.4.3.1.7 Time (ID 7)

a) The bit format of the Time parameter **shall**[97] be encoded/decoded as indicated in Figure 3-9.

<table>
<tr><td></td><td>First bit Trans-mitted</td><td colspan="7">Bit Number</td></tr>
<tr><td>Octet</td><td>1</td><td>2</td><td>3</td><td>4</td><td>5</td><td>6</td><td>7</td><td>8</td></tr>
<tr><td>1</td><td colspan="4">Month</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>2</td><td colspan="5">Day</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>3</td><td colspan="8">Year-2000</td></tr>
<tr><td>4</td><td colspan="5">Hours</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>5</td><td colspan="6">Minutes</td><td>0</td><td>0</td></tr>
<tr><td>6</td><td colspan="8" rowspan="2">Seconds*100</td></tr>
<tr><td>7</td></tr>
</table>

- Month field has a range of 1 to 12 for January to December.
- Day field has a range of 1 to 31.
- Year-2000 field has an offset of 2000, (i.e., year 2000 is encoded as 0).
- Hours field has a range of 0 to 23.
- Minutes field has a range of 0 to 59.
- Seconds*100 field has a range of 0 to 5999 (which corresponds to 0.00 to 59.99 seconds).

Figure 3-9. Time Parameter Format

3.2.2.1.4.3.1.8 Squelch RF Threshold Level Setting (AM) (ID 8)

a) The bit format of the Squelch RF Threshold Level Setting parameter **shall**[99] be encoded/decoded as indicated in Figure 3-10.

	First bit Trans-mitted	Bit Number						
Octet	1	2	3	4	5	6	7	8
1	Squelch RF Threshold Level Setting						0	0

- Squelch RF Threshold Level Setting has a valid range of 0 to 63 corresponding to discrete settings of RF input power levels in the range of -102 to -50 dBm.

Figure 3-10. Squelch RF Threshold Level Setting Parameter Format

3.2.2.1.4.3.1.9 Squelch Audio Signal-to-Noise Level Setting (ID 9)

a) The bit format of the Squelch Audio Signal-to-Noise Level Setting parameter **shall**[272] be encoded/decoded as indicated in Figure 3-11.

	First bit Trans-mitted	Bit Number						
Octet	1	2	3	4	5	6	7	8
1	Squelch Audio Signal-to-Noise Level Setting				0	0	0	0

- Squelch Audio Signal-to-Noise Level Setting has a valid range of 0 to 10 corresponding to discrete settings of audio signal-to-noise ratio in the range of +5 to +15 dBm.

Figure 3-11. Squelch Audio Signal-to-Noise Level Setting Parameter Format

3.2.2.1.4.3.1.10 Audio Output Level (AM) (ID 10)

a) The bit format of the Audio Output Level parameter **shall**[103] be encoded/decoded as indicated in Figure 3-12.

	First bit Trans-mitted	Bit Number						
Octet	1	2	3	4	5	6	7	8
1	AudioLevel+25						0	0

- Where AudioLevel+25 dBm means that -25 dBm is encoded as 0 and +20.0 dBm is encoded as 45.

Figure 3-12. Audio Output Level Parameter Format

3.2.2.1.4.3.1.11 Receiver Mute (AM) (ID 11)

a) The bit format of the Receiver Mute parameter **shall**[105] be encoded/decoded as indicated in Figure 3-13.

	First bit Trans-mitted	Bit Number						
Octet	1	2	3	4	5	6	7	8
1	ReceiverMute							

- Where ReceiverMute is encoded/decoded as follows:
  0 = Unmuted
  255 = Muted

Figure 3-13. Receiver Mute Parameter Format

3.2.2.1.4.3.1.12 Power Output (AM) (ID 12)

a) The bit format of the Power Output parameter **shall**[107] be encoded/decoded as indicated in Figure 3-14.

	First bit Trans-mitted	Bit Number						
Octet	1	2	3	4	5	6	7	8
1	PowerOutput Setting						0	0

- The PowerOutput Setting field is encoded as:
  desired power output (dBm)*2 - 60.
- Since the valid range for desired power output is as follows:
  - from 33dBm - 42dBm in 0.5dB increments for 15W transmitter
  - from 40dBm - 47dBm in 0.5dB increments for 50W transmitter, and
  - from 33dBm - 47dBm in 0.5dB increments if a single transmitter is used to fulfill both 15W and 50W transmitter requirements,

  the PowerOutput Setting field has a valid range of
  - 6 to 24 for 15W transmitter
  - 20 to 34 for 50W transmitter, and
  - 6 to 34 if a single transmitter is used to fulfill both 15W and 50W transmitter requirements.

Figure 3-14. Power Output Parameter Format

3.2.2.1.4.3.1.13 Transmitter Modulation % (AM) (ID 13)

a) The bit format of the Transmitter Modulation % parameter **shall**[109] be encoded/decoded as indicated in Figure 3-15.

	First bit Trans-mitted	Bit Number						
Octet	1	2	3	4	5	6	7	8
1	Transmitter Modulation %							0

- Where Transmitter Modulation % is linearly encoded/decoded for 0 – 100% in steps of 1

Figure 3-15. Transmitter Modulation % Parameter Format

3.2.2.1.4.3.1.14 ATR Switch State (ID 14)

a) The bit format of the ATR Switch State parameter **shall**[121] be encoded/decoded as indicated in Figure 3-16.

	First bit Trans-mitted	Bit Number						
Octet	1	2	3	4	5	6	7	8
1	ATR Switch State							

- Where ATR Switch State is encoded/decoded as follows:
  0 = ATR2
  255 = ATR1

Figure 3-16. ATR Switch State Parameter Format

3.2.2.1.4.3.1.15 Switch Software Version (ID 15)

a) The bit format of the Switch Software Version parameter **shall**[129] be encoded/decoded as indicated in Figure 3-17.

	First bit Trans-mitted	Bit Number						
Octet	1	2	3	4	5	6	7	8
1	Switch Software (0=Switch Software version)							

Figure 3-17. Switch Software Version Parameter Format

3.2.2.1.4.3.1.16 N1 (Number of Information Bits) (ID 16)

a) The bit format of the N1 parameter **shall**[135] be encoded/decoded as indicated in Figure 3-18.

	First bit Trans-mitted	Bit Number						
Octet	1	2	3	4	5	6	7	8
1	(msb)				Reserved			
2	(lsb) N1-1 (bits)							

- Where N1-1 is encoded/decoded linearly from 127 to 4095 (which corresponds to a range of 128 to 4096 bits).

Figure 3-18. N1 Parameter Format

3.2.2.1.4.3.1.17 T1 (Link Response Timer) (ID 17)

a) The bit format of the T1 parameter **shall**[137] be encoded/decoded as indicated in Figure 3-19.

	First bit Trans-mitted	Bit Number						
Octet	1	2	3	4	5	6	7	8
1	(msb)	Reserved						
2	(lsb)	T1 (ms)						

Figure 3-19. T1 Parameter Format

3.2.2.1.4.3.1.18 T3 (Reassembly Timer) (ID 18)

a) The bit format of the T3 parameter **shall**[139] be encoded/decoded as indicated in Figure 3-20.

	First bit Trans-mitted	Bit Number						
Octet	1	2	3	4	5	6	7	8
1	T3 (ms)							(msb)
2	(lsb)							

Figure 3-20. T3 Parameter Format

3.2.2.1.4.3.1.19 HDLC Channel Number (ID 19)

a) The bit format of the HDLC Channel Number Parameter **shall**[251] be encoded/decoded as indicated in Figure 3-21.

	First bit Trans-mitted	Bit Number						
Octet	1	2	3	4	5	6	7	8
1	Channel Number			0	0	0	0	0

Figure 3-21. HDLC Channel Number Parameter Format

3.2.2.1.4.3.1.20 Transmission Timeout (AM) (ID 20)

a) The bit format of the Transmission Timeout parameter **shall**[111] be encoded/decoded as indicated in Figure 3-22.

	First bit Trans-mitted	Bit Number						
Octet	1	2	3	4	5	6	7	8
1	TIMEOUT/5 (0=Disabled)						0	0

- Where TIMEOUT/5 is encoded in 5 sec steps, such that 5 sec is encoded as 1, 10 sec is encoded as 2 and so forth.
- The transmission timeout parameter is disabled by setting the field to zero.

Figure 3-22. Transmission Timeout Parameter Format

3.2.2.1.4.3.1.21 Squelch Enable/Disable (AM) (ID 21)

a) The bit format of the Squelch Enable/Disable parameter **shall**[252] be encoded/decoded as indicated in Figure 3-23.

	First bit Trans-mitted	Bit Number						
Octet	1	2	3	4	5	6	7	8
1	Squelch Enable/Disable							

- Where Squelch Enable/Disable is encoded/decoded as follows:
  0 = Disable
  255 = Enable

Figure 3-23. Squelch Enable/Disable Parameter Format

3.2.2.1.4.3.1.22 ATR Switch Mode (ID 22)

a) The bit format of the ATR Switch Mode parameter **shall**[294] be encoded/decoded as indicated in Figure 3-24.

	First bit Trans-mitted	Bit Number						
Octet	1	2	3	4	5	6	7	8
1	Switch Mode							

- Where Switch Mode is encoded/decoded as follows:
  0 = Static
  255 = Dynamic

Figure 3-24. ATR Switch Mode Parameter Format

3.2.2.1.4.3.1.23 Request Read Back (ID 30)

a) The bit format of the Request Read Back parameter **shall**[95] be encoded/decoded as indicated in Figure 3-25a.

	First bit Trans-mitted	Bit Number						
Octet	1	2	3	4	5	6	7	8
1	Monitor ID							Type
2	Iterations							
3	Interval							
4	Filter				0	0	0	0
5	Data							
6								
7								
8								
9								

- Monitor ID is the ID of the monitoring parameter being requested.
- Type specifies the request readback type.
  - 0 = Monitoring values are requested,
  - 1 = Alert and alarm threshold values are requested.
- Iterations field is the number of readbacks requested. 255 is reserved to indicate continuous sending (at the specified interval) until commanded to cease. 0 is used to command to cease.
- Interval specifies the spacing between reporting of the parameters measured in 240 ms cycles.
- For monitoring parameters with non-iterating readbacks, the Iterations field is set to 1 and the Interval field is set to 0.
- The Filter field is encoded according to Table 3-2.
- The Data field is encoded according to Figure 3-25b and 3-25c.

Figure 3-25a. Request Read Back Parameter Format

Table 3-2. Request Read Back Filter Encoding

Filter Condition	Data Field	Filter Value	Data Field Format
All	-	0000	All zeros
All	Date/Time	0000	Figure 3-25b
State Change	-	0001	All zeros
State Change	Date/Time	0001	Figure 3-25b
Control	-	0010	All zeros
Control-DT	Date/Time	0010	Figure 3-25b
Control-ID	ID	0011	Figure 3-25c
Failure	-	0100	All zeros
Alarm/Alert/RTN	-	0101	All zeros
Alarm/Alert/RTN-DT	Date/Time	0101	Figure 3-25b
Alarm/Alert/RTN-ID	ID	0110	Figure 3-25c
Log-In/Log-Out	-	0111	All zeros
Log-In/Log-Out-DT	Date/Time	0111	Figure 3-25b

	First bit Trans-mitted	Bit Number						
Octet	1	2	3	4	5	6	7	8
5	Month				0	0	0	0
6	Day					0	0	0
7	Year-2000							
8	Hours					0	0	0
9	Minutes						0	0

- Month field has a range of 1 to 12 for January to December.
- Day field has a range of 1 to 31.
- Year-2000 field has an offset of 2000 (i.e., year of 2000 is encoded as 0).
- Hours field has a range of 0 to 23.
- Minutes field has a range of 0 to 59.

Figure 3-25b. Request Readback Parameter, Data Field Format for Time Filter

	First bit Trans-mitted	Bit Number						
Octet	1	2	3	4	5	6	7	8
5	Monitor ID							0
6	0	0	0	0	0	0	0	0
7	0	0	0	0	0	0	0	0
8	0	0	0	0	0	0	0	0
9	0	0	0	0	0	0	0	0

- Monitor ID is the ID of the monitoring parameter being requested.

Figure 3-25c. Request Readback Parameter, Data Field Format for ID Filter

3.2.2.1.4.3.1.24 Audio Input Level (AM) (ID 31)

a) The bit format of the Audio Input Level parameter **shall**[113] be encoded/decoded as indicated in Figure 3-26.

	First bit Trans-mitted	Bit Number						
Octet	1	2	3	4	5	6	7	8
1	AudioInputLevel Setting							0

- The AudioInputLevel Setting field is encoded as follows:
  expected Audio Input Level (in dBm)*2 + 50.
- Since the expected Audio Input Level has a range of -25.0 to +20.0 dBm, in 0.5 dBm steps, the AudioInputLevel Setting field has a valid range of 0 to 90.

Figure 3-26. Audio Input Level Parameter Format

3.2.2.1.4.3.1.25 Reserved (ID 32)

3.2.2.1.4.3.1.26 Reserved (ID 33)

3.2.2.1.4.3.1.27 MAC Timing Offset Correction (VDL Mode 3) (ID 34)

a) The bit format of the MAC Timing Offset Correction parameter **shall**[119] be encoded/decoded as indicated in Figure 3-27.

	First bit Trans-mitted	Bit Number						
Octet	1	2	3	4	5	6	7	8
1	Time Offset (in μs)							(msb)
2	(lsb)	(2's Complement Format)						

- Time Offset is encoded/decoded as a 2's complement format with a range of –32768 to 32767.

Figure 3-27. MAC Timing Offset Correction Parameter Format

3.2.2.1.4.3.1.28 Suppress Alert/Alarm (ID 35)

a) The bit format of the Suppress Alert/Alarm parameter **shall**[123] be encoded/decoded as indicated in Figure 3-28.

	First bit Trans-mitted	Bit Number						
Octet	1	2	3	4	5	6	7	8
1	Suppress Alert/Alarm							

- Where Suppress Alert/Alarm is encoded/decoded as follows:
  0 = Normal
  255 = Suppress

Figure 3-28. Suppress Alert/Alarm Parameter Format

3.2.2.1.4.3.1.29 Reset (ID 36)

a) The bit format of the Reset parameter **shall**[125] be encoded/decoded as indicated in Figure 3-29.

	First bit Trans-mitted	Bit Number						
Octet	1	2	3	4	5	6	7	8
1	Reset							

- Where Reset is encoded/decoded as follows:
  0 = Warm Reset
  255 = Factory Reset

Figure 3-29. Reset Parameter Format

3.2.2.1.4.3.1.30 Software Upload Enable/Disable (ID 37)

a) The bit format of the Software Upload Enable/Disable parameter **shall**[127] be encoded/decoded as indicated in Figure 3-30.

	First bit Trans-mitted	Bit Number						
Octet	1	2	3	4	5	6	7	8
1	Upload							

- Where Upload is encoded/decoded as follows:
  0 = Enable
  255 = Disable

Figure 3-30. Software Upload Enable/Disable Parameter Format

3.2.2.1.4.3.1.31 Software Upload (ID 38)

a) The bit format of the Software Upload parameter **shall**[131] be encoded/decoded as indicated in Figure 3-31.

	First bit Trans-mitted	Bit Number						
Octet	1	2	3	4	5	6	7	8
1	Block Number							(msb)
2	(lsb)							
3	Total Blocks							(msb)
4	(lsb)							
5	Program Binary Block							
6								
7+	(Up to 432 Bits (54 octets))							

- Total Blocks field indicates the total number of data blocks expected to receive.
- Block Number field is the current block number and has a range of 1 to Total Blocks.
- Program Binary Block(s) contain the binary image of new software, and a digital signature (of the binary image of the new software) in the last 1, 2, or 3 delivered program binary blocks (depending upon the implementation-specific size of the digital signature).

Figure 3-31. Software Upload Parameter Format

3.2.2.1.4.3.1.32 Receiver Mute Level (AM) (ID 39)

a) The bit format of the Receiver Mute Level parameter **shall**[253] be encoded/decoded as indicated in Figure 3-32.

	First bit Trans-mitted	Bit Number						
Octet	1	2	3	4	5	6	7	8
1	Mute Level							

- Where Mute Level is encode/decoded as follows:
  0 = -15 dB
  85 = -20 dB
  255 = No Audio.

Figure 3-32. Receiver Mute Level Parameter Format

3.2.2.1.4.3.1.33 Test PTT (AM) (ID 40)

a) The bit format of the Test PTT parameter **shall**[254] be encoded/decoded as indicated in Figure 3-33.

	First bit Trans-mitted	Bit Number						
Octet	1	2	3	4	5	6	7	8
1	Test PTT							

- Where Test PTT is encoded/decoded as follows:
  0 = Not_Test_Keyed
  255 = Test_Keyed

Figure 3-33. Test PTT Parameter Format

3.2.2.1.4.3.1.34 Public Key Maintenance (ID 41)

a) The bit format of the Public Key Maintenance parameter **shall**[273] be encoded/decoded as indicated in Figure 3-34.

	First bit Trans-mitted	Bit Number						
Octet	1	2	3	4	5	6	7	8
1	Month				0	0	0	0
2	Day					0	0	0
3	Year-2000							
4	Hours					0	0	0
5	Minutes						0	0
6 ... 25	User ID							
26 ... 65	Terminal ID							
66	Key Action							
67	Key ID (0 - 9)							
68 ... Y*	(msb) Public Key (lsb)							
Y*+1 ... Z**	(msb) Security Token (lsb)							

- Month, Day, Year, Hours and Minutes fields are encoded as specified in 3.2.2.1.4.3.1.7.
- User ID and Terminal ID fields are encoded as specified in 3.2.2.1.4.3.1.1.
- Key Action field is encoded as follows:
  0 = Add Key
  1-254 = RESERVED
  255 = Delete Key
  Key ID field has a valid range of 0 to 9
- Y*: Size of public key is implementation specific and determined by the vendor, in accordance with FAA-E-2928, Section 3.2.3.9.
- Z**: Security Token size is implementation specific, as specified in Section 3.2.2.1.4.3.1.1.

Figure 3-34. Public Key Maintenance Parameter Format

3.2.2.1.4.3.1.35 T2 (Link Retransmission Timer) (ID 42)

a) The bit format of the T2 parameter **shall**[274] be encoded/decoded as indicated in Figure 3-35.

	First bit Trans-mitted	Bit Number						
Octet	1	2	3	4	5	6	7	8
1	T2				0	0	0	0

- T2 field has a range of 1 to 10 with a step size of 1.

Figure 3-35. T2 Parameter Format

3.2.2.1.4.3.2 MDR Monitoring Parameters

a) The MDR will support the monitoring parameters identified in Table 3-1. The attributes of the monitoring parameters are defined in FAA-E-2938.
b) The bit formats of the monitoring packets (Refer to section 3.2.2.6.5.1.7) are defined in sections 3.2.2.1.4.3.2.1 through 3.2.2.1.4.3.2.44. The ID number in Table 3-1 corresponds to the CTYPE field defined in the general message structure format.
c) The PID field is set to all zeros to use the following bit formats. For each octet, bit 1 is the lsb and bit 8 is msb. Lower numbered octets contain higher order bits for fields that cross octet boundaries. Reserved fields are all zeroes.

3.2.2.1.4.3.2.1 Event Log (ID 1)

a) The bit format of the Event Log parameter **shall**[54] be encoded/decoded as indicated in Figure 3-36.

	First bit Transmitted	Bit Number						
Octet	1	2	3	4	5	6	7	8
1	Event Log Msg ID							
2	Month				0	0	0	0
3	Day					0	0	0
4	Year-2000							
5	Hours					0	0	0
6	Minutes						0	0
7	MDR ID							
8								
9								
10	Filter				0	0	0	0
11	Data							
12								
13								
14								
15								
16	Number of Log Entries (in this Event Log Entries field)							
17	Event Log Entries							
...								
+								

- Transmission of all Event Log Entries that match the Request Readback criteria may require a series of (more than 1) Event Log messages.
- Event Log Msg ID field contains a binary counter that identifies the Event Log message in the series, and has a range of 1 - 255.
- Month, Day, Year, Hour and Minute fields are encoded as specified in 3.2.2.1.4.3.1.7.
- MDR ID is encoded as a binary number, and has a range of 1 to 16777215.
- Filter and Data fields are encoded per Section 3.2.2.1.4.3.1.23, and include the same information contained in the Request Readback message that initiated the Event Log Readback.
- Number of Log Entries field contains a binary value indicating number of event log entries contained in the Event Log Entries field, from 0 - 255.
- Event Log Entries field is comprised of any mixture of the six types of event log entry data, (in implementation specific format), in accordance with FAA-E-2938.
- The Day/Time subfield of each Event Log Entry in the Event Log Entries field requires the "Seconds" field to achieve desired resolution down to a MAC cycle.

Figure 3-36. Event Log Parameter Format

3.2.2.1.4.3.2.2 Current Frequency (ID 2)

a) The bit format of the Current Frequency parameter **shall**[36] be encoded/decoded as indicated in Figure 3-37.

	First bit Trans-mitted	Bit Number						
Octet	1	2	3	4	5	6	7	8
1	FrequencyID							(msb)
2	(lsb)							

- FrequencyID is encoded as INT((F*1000-112000) / 8.333) where F is the desired frequency in MHz, expressed with eight significant digits (e.g. 132.00833).
- The INT(x) function yields the integer value of x.
- The frequency begins at 112 MHz and increases in steps of 8 1/3 kHz
- The FrequencyID represents how many 8 1/3 kHz steps above 112 MHz the Frequency is.
- Frequency ID has a valid range of 0 to 2997 in increments of 1.
- The following example illustrates the Frequency and FrequencyID mapping:

Valid FrequencyID for Current Frequency	Frequency
0	112.00000
1	112.00833
2	112.01667
3	112.02500
4	112.03333
5	112.04167
6	112.05000
7	112.05833
8	112.06667
9	112.07500
10	112.08333
11	112.09167
12	112.10000
....	...

Figure 3-37. Current Frequency Parameter Format

3.2.2.1.4.3.2.3 Lowest Tunable Frequency (ID 3)

a) The bit format of the Lowest Tunable Frequency parameter **shall**[8] be encoded/decoded as indicated in Figure 3-38.

	First bit Trans- mitted	Bit Number						
Octet	1	2	3	4	5	6	7	8
1	LT_FrequencyID							(msb)
2	(lsb)							

- LT_FrequencyID is encoded as INT((F*1000-112000) / 8.333) where F is the desired frequency in MHz, expressed with eight significant digits (e.g. 112.02500).
- The INT(x) function yields the integer value of x.
- For the Lowest Tunable Frequency parameter, the frequency F begins at 112 MHz and increases in steps of 25 kHz.
- LT_FrequencyID has a valid range of 0 to 2997 in increments of 3.
- The following example illustrates the Frequency and LT_FrequencyID mapping:

Valid LT_FrequencyID for Lowest Tunable Frequency	Frequency
0	112.00000
3	112.02500
6	112.05000
9	112.07500
12	112.10000
....	...

Figure 3-38. Lowest Tunable Frequency Parameter Format

3.2.2.1.4.3.2.4 Mode of Operation (ID 4)

a) The bit format of the Mode of Operation parameter **shall**[34] be encoded/decoded as indicated in Figure 3-39.

	First bit Trans-mitted	Bit Number						
Octet	1	2	3	4	5	6	7	8
1	MODE							

- Where MODE is encoded as follows:
  0 = 25kHz DSB-AM
  85 = 8.33kHz DSB-AM
  255 = VDL Mode 3

Figure 3-39. Mode of Operation Parameter Format

3.2.2.1.4.3.2.5 MDR State (ID 5)

a) The bit format of the MDR State parameter **shall**[4] be encoded/decoded as indicated in Figure 3-40.

	First bit Trans-mitted	Bit Number						
Octet	1	2	3	4	5	6	7	8
1	STATE			Reserved				

- Where STATE is encoded as follows:
  0 = OFFLINE
  1 = POWER DOWN (if exercised)
  2 = POWER UP
  3 = ONLINE
  4-5 = Reserved
  6 = RECOVERY (Cannot be remotely controlled to this state)
  7 = FAIL (Cannot be remotely controlled to this state)

Figure 3-40. MDR State Parameter Format

3.2.2.1.4.3.2.6 Threshold Setting (ID 6)

a) The bit format of the Threshold Setting parameter **shall**[255] be encoded/decoded as indicated in Figure 3-41.

	First bit Trans-mitted	Bit Number						
Octet	1	2	3	4	5	6	7	8
1	(lsb)			Monitor ID				(msb)
2				Low Alert Threshold				(msb)
3	(lsb)							
4				High Alert Threshold				(msb)
5	(lsb)							
6				Low Alarm Threshold				(msb)
7	(lsb)							
8				High Alarm Threshold				(msb)
9	(lsb)							

- Monitor ID field indicates the particular monitoring parameter ID to which the following alert and alarm thresholds apply.
- Alert and Alarm Thresholds are encoded/decoded according to Section 3.2.2.1.4.3.1.6.
- If a particular monitoring parameter has only one threshold, then the other threshold value is set to zero.

Figure 3-41. Threshold Setting Parameter Format

3.2.2.1.4.3.2.7 Time (ID 7)

a) The bit format of the Time parameter **shall**[38] be encoded/decoded as indicated in Figure 3-42.

	First bit Trans-mitted	Bit Number					
Octet	1	2	3	4	5	6	7	8
1	Month				0	0	0	0
2	Day					0	0	0
3	Year-2000							
4	Hours					0	0	0
5	Minutes						0	0
6	Seconds*100							
7								

- Month field has a range of 1 to 12 for January to December.
- Day field has a range of 1 to 31.
- Year-2000 field has an offset of 2000 (i.e., year 2000 is encoded as 0).
- Hours field has a range of 0 to 23.
- Minutes field has a range of 0 to 59.
- Seconds*100 field has a range of 0 to 5999 (which corresponds to 0.00 to 59.99 seconds).

Figure 3-42. Time Parameter Format

3.2.2.1.4.3.2.8 Squelch RF Threshold Level Setting (AM) (ID 8)

a) The bit format of the Squelch RF Threshold Level Setting parameter **shall**[28] be encoded/decoded as indicated in Figure 3-43.

	First bit Trans-mitted	Bit Number						
Octet	1	2	3	4	5	6	7	8
1	Squelch RF Threshold Level Setting						0	0

- Squelch RF Threshold Level Setting has a range of 0 to 63 corresponding to discrete settings of RF input power levels in the range of -102 to -50 dBm.

Figure 3-43. Squelch RF Threshold Level Setting Parameter Format

3.2.2.1.4.3.2.9 Squelch Audio Signal-to-Noise Level Setting (ID 9)

a) The bit format of the Squelch Audio Signal-to-Noise Level Setting parameter **shall**[275] be encoded/decoded as indicated in Figure 3-44.

	First bit Trans-mitted	Bit Number						
Octet	1	2	3	4	5	6	7	8
1	Squelch Audio Signal-to-Noise Level Setting				0	0	0	0

- Squelch Audio Signal-to-Noise Level Setting has a range of 0 to 10 corresponding to discrete settings of audio signal-to-noise ratio in the range of +5 to +15 dBm.

Figure 3-44. Squelch Audio Signal-to-Noise Level Setting Parameter Format

3.2.2.1.4.3.2.10 Audio Output Level (AM) (ID 10)

a) The bit format of the Audio Output Level parameter **shall**[48] be encoded/decoded as indicated in Figure 3-45.

	First bit Trans-mitted	Bit Number						
Octet	1	2	3	4	5	6	7	8
1	AudioLevel+25						0	0

- Where AudioLevel+25 dBm means that -25 dBm is encoded as 0 and +20.0 dBm is encoded as 45.

Figure 3-45. Audio Output Level Parameter Format

3.2.2.1.4.3.2.11 Receiver Mute (AM) (ID 11)

a) The bit format of the Receiver Mute parameter **shall**[44] be encoded/decoded as indicated in Figure 3-46.

	First bit Trans-mitted	Bit Number						
Octet	1	2	3	4	5	6	7	8
1	ReceiverMute							

- Where ReceiverMute is encoded/decoded as follows:
  0 = Unmuted
  255 = Muted

Figure 3-46. Receiver Mute Parameter Format

3.2.2.1.4.3.2.12 Power Output Setting (AM) (ID 12)

a) The bit format of the Power Output Setting parameter **shall**[16] be encoded/decoded as indicated in Figure 3-47.

	First bit Trans-mitted	Bit Number					
Octet	1	2	3	4	5	6	7	8
1	PowerOutput Setting						0	0

- The PowerOutput Setting field is encoded as:
  desired power output (dBm)*2 - 60.
- Since the valid range for desired power output is as follows:
  - from 33dBm - 42dBm in 0.5dB increments for 15W transmitter
  - from 40dBm - 47dBm in 0.5dB increments for 50W transmitter, and
  - from 33dBm - 47dBm in 0.5dB increments if a single transmitter is used to fulfill both 15W and 50W transmitter requirements,

  the PowerOutput Setting field has a valid range of
  - 6 to 24 for 15W transmitter
  - 20 to 34 for 50W transmitter, and
  - 6 to 34 if a single transmitter is used to fulfill both 15W and 50W transmitter requirements.

Figure 3-47. Power Output Setting Parameter Format

3.2.2.1.4.3.2.13 Transmitter Modulation % Setting (AM) (ID 13)

a) The bit format of the Transmitter Modulation % Setting parameter **shall**[18] be encoded/decoded as indicated in Figure 3-48.

	First bit Trans-mitted	Bit Number						
Octet	1	2	3	4	5	6	7	8
1	Modulation %							0

- Where Modulation % is linearly encoded/decoded for 0 – 100% in steps of 1.

Figure 3-48. Transmitter Modulation % Setting Parameter Format

3.2.2.1.4.3.2.14 ATR Switch State (ID 14)

a) The bit format of the ATR Switch State parameter **shall**[69] be encoded/decoded as indicated in Figure 3-49.

	First bit Trans-mitted	Bit Number						
Octet	1	2	3	4	5	6	7	8
1	ATR Switch State							

- Where ATR Switch State is encoded/decoded as follows:
  0 = ATR2
  255 = ATR1

Figure 3-49. ATR Switch State Parameter Format

3.2.2.1.4.3.2.15 Software Version (ID 15)

a) The bit format of the Software Version parameter **shall**[2] be encoded/decoded as indicated in Figure 3-50.

	First bit Trans-mitted	Bit Number						
Octet	1	2	3	4	5	6	7	8
1	Current Version							
2	Standby Version							

- Both fields have a range of 1 to 255.
- A value of 0 is used for invalid or non-existent version.

Figure 3-50. Software Version Parameter Format

3.2.2.1.4.3.2.16 N1 (Number of Information Bits) (ID 16)

a) The bit format of the N1 parameter **shall**[75] be encoded/decoded as indicated in Figure 3-51.

	First bit Trans-mitted	Bit Number						
Octet	1	2	3	4	5	6	7	8
1				(msb)	Reserved			
2	(lsb)			N1-1	(bits)			

- Where N1-1 is encoded/decoded linearly from 127 to 4095 (which corresponds to a range of 128 to 4096 bits).

Figure 3-51. N1 Parameter Format

3.2.2.1.4.3.2.17 T1 (Link Response Timer) (ID 17)

a) The bit format of the T1 parameter **shall**[77] be encoded/decoded as indicated in Figure 3-52.

	First bit Trans-mitted	Bit Number						
Octet	1	2	3	4	5	6	7	8
1	(msb)	Reserved						
2	(lsb)	T1 (ms)						

Figure 3-52. T1 Parameter Format

3.2.2.1.4.3.2.18 T3 (Reassembly Timer) (ID 18)

a) The bit format of the T3 parameter **shall**[79] be encoded/decoded as indicated in Figure 3-53.

	First bit Trans-mitted	Bit Number						
Octet	1	2	3	4	5	6	7	8
1	T3 (ms)							(msb)
2	(lsb)							

Figure 3-53. T3 Parameter Format

3.2.2.1.4.3.2.19 HDLC Channel Number (ID 19)

a) The bit format of the HDLC Channel Number Parameter **shall**[256] be encoded/decoded as indicated in Figure 3-54.

	First bit Trans-mitted	Bit Number						
Octet	1	2	3	4	5	6	7	8
1	Channel Number			0	0	0	0	0

Figure 3-54. HDLC Channel Number Parameter Format

3.2.2.1.4.3.2.20 Transmission Timeout Setting (AM) (ID 20)

a) The bit format of the Transmission Timeout Setting parameter **shall**[14] be encoded/decoded as indicated in Figure 3-55.

	First bit Trans-mitted	Bit Number						
Octet	1	2	3	4	5	6	7	8
1	TIMEOUT/5 (0=Disabled)						0	0

- Where TIMEOUT/5 is encoded in 5 sec steps, such that 5 sec is encoded as 1, 10 sec is encoded as 2 and so forth.
- The transmission timeout parameter is disabled by setting the field to zero.

Figure 3-55. Transmission Timeout Setting Parameter Format

3.2.2.1.4.3.2.21 Squelch Enable/Disable (AM) (ID 21)

a) The bit format of the Squelch Enable/Disable parameter **shall**[24] be encoded/decoded as indicated in Figure 3-56.

	First bit Trans-mitted	Bit Number						
Octet	1	2	3	4	5	6	7	8
1	Squelch Enable/Disable							

- Where Squelch Enable/Disable is encoded/decoded as follows:
  0 = Disable
  255 = Enable

Figure 3-56. Squelch Enable/Disable Parameter Format

3.2.2.1.4.3.2.22 ATR Switch Mode (ID 22)

a) The bit format of the ATR Switch Mode parameter **shall**[295] be encoded/decoded as indicated in Figure 3-57.

	First bit Trans-mitted	Bit Number						
Octet	1	2	3	4	5	6	7	8
1	Switch Mode							

- Where Switch Mode is encoded/decoded as follows:
  0 = Static
  255 = Dynamic

Figure 3-57. ATR Switch Mode Parameter Format

3.2.2.1.4.3.2.23 RESERVED (ID 30)

3.2.2.1.4.3.2.24 Audio Input Level Setting (ID 31)

a) The bit format of the Audio Input Level Setting parameter **shall**[276] be encoded/decoded as indicated in Figure 3-58.

	First bit Trans-mitted	Bit Number						
Octet	1	2	3	4	5	6	7	8
1	AudioInputLevel Setting							0

- The AudioInputLevel Setting field is encoded as follows:
  expected Audio Input Level (in dBm)*2 + 50.
- Since the expected Audio Input Level has a range of -25.0 to +20.0 dBm, in 0.5 dBm steps, the AudioInputLevel Setting field has a valid range of 0 to 90.

Figure 3-58. Audio Input Level Setting Parameter Format

3.2.2.1.4.3.2.25 RESERVED (ID 32)

3.2.2.1.4.3.2.26 RESERVED (ID 33)

3.2.2.1.4.3.2.27 MAC Timing Offset Correction (VDL Mode 3) (ID 34)

a) The bit format of the MAC Timing Offset Correction parameter **shall**[277] be encoded/decoded as indicated in Figure 3-59.

	First bit Trans-mitted	Bit Number						
Octet	1	2	3	4	5	6	7	8
1	Time Offset (in us) (msb)							
2	(lsb) (2's Complement Format)							

- Time Offset is encoded/decoded as a 2's complement format with a range of -32768 to 32767.

Figure 3-59. MAC Timing Offset Correction Parameter Format

3.2.2.1.4.3.2.28 Suppress Alarm/Alert Setting (ID 35)

a) The bit format of the Suppress Alert/Alarm Setting parameter **shall**[278] be encoded/decoded as indicated in Figure 3-60.

	First bit Trans-mitted	Bit Number						
Octet	1	2	3	4	5	6	7	8
1	Suppress Alert/Alarm							

- Where Suppress Alert/Alarm is encoded/decoded as follows:
  0 = Normal
  255 = Suppress

Figure 3-60. Suppress Alert/Alarm Setting Parameter Format

3.2.2.1.4.3.2.29 RESERVED (ID 36)

3.2.2.1.4.3.2.30 Software Upload Setting (ID 37)

a) The bit format of the Software Upload Setting parameter **shall**[279] be encoded/decoded as indicated in Figure 3-61.

	First bit Trans-mitted	Bit Number						
Octet	1	2	3	4	5	6	7	8
1	Upload							

- Where Upload is encoded/decoded as follows:
  0 = Enable
  255 = Disable

Figure 3-61. Software Upload Setting Parameter Format

3.2.2.1.4.3.2.31 RESERVED (ID 38)

3.2.2.1.4.3.2.32 Receiver Mute Level Setting (ID 39)

a) The bit format of the Receiver Mute Level Setting parameter **shall**[280] be encoded/decoded as indicated in Figure 3-62.

	First bit Trans-mitted	Bit Number						
Octet	1	2	3	4	5	6	7	8
1	Mute Level							

- Mute Level is encoded/decoded as follows:
  0 = -15 dB
  85 = -20 dB
  255 = No Audio.

Figure 3-62. Receiver Mute Level Setting Parameter Format

3.2.2.1.4.3.2.33 PTT Setting (ID 40)

a) The bit format of the PTT Setting parameter **shall**[281] be encoded/decoded as indicated in Figure 3-63.

	First bit Trans-mitted	Bit Number						
Octet	1	2	3	4	5	6	7	8
1	PTT Setting							

- Where PTT Setting is encoded/decoded as follows:
  0 = Not_Test_Keyed
  85 = User_Keyed
  255 = Test_Keyed

Figure 3-63. PTT Setting Parameter Format

3.2.2.1.4.3.2.34 Public Key List (ID 41)

a) The bit format of the Public Key List parameter **shall**[282] be encoded/decoded as indicated in Figure 3-64.

	First bit Trans-mitted	Bit Number						
Octet	1	2	3	4	5	6	7	8
1	Month				0	0	0	0
2	Day					0	0	0
3	Year-2000							
4	Hours					0	0	0
5	Minutes						0	0
6	MDR ID							(msb)
7								
8	(lsb)							
9	Key ID (0-9)				0	0	0	0
10	Public Key							(msb)
...								
10+A*	(lsb)							

11+A	Key ID (0-9)	0	0	0	0
12+A	(msb)				
...	Public Key				
12+2A	(lsb)				
13+2A	Key ID (0-9)	0	0	0	0
14+2A	(msb)				
...	Public Key				
14+3A	(lsb)				
15+3A	Key ID (0-9)	0	0	0	0
16+3A	(msb)				
...	Public Key				
16+4A	(lsb)				
17+4A	Key ID (0-9)	0	0	0	0
18+4A	(msb)				
...	Public Key				
18+5A	(lsb)				
19+5A	Key ID (0-9)	0	0	0	0
...	(msb)				
19+6A	Public Key				
20+6A	(lsb)				
21+6A	Key ID (0-9)	0	0	0	0
22+6A	(msb)				
...	Public Key				
22+7A	(lsb)				
23+7A	Key ID (0-9)	0	0	0	0
24+7A	(msb)				
...	Public Key				
24+8A	(lsb)				
25+8A	Key ID (0-9)	0	0	0	0
26+8A	(msb)				
...	Public Key				
26+9A	(lsb)				
27+9A	Key ID (0-9)	0	0	0	0
28+9A	(msb)				
...	Public Key				
28+10A	(lsb)				

- Month, Day, Year, Hours and Minutes fields are encoded as specified in 3.2.2.1.4.3.1.7.

- MDR ID field is encoded as specified in 3.2.2.1.4.3.2.36.
- If the Public Key associated with a Public Key ID is not established (null), the MDR would not send (would skip) the Key ID field octet and its associated Public Key field octets.
- A*: Size of Public Key is implementation specific and determined by the vendor, in accordance with FAA-E-2938, Section 3.2.3.9.

Figure 3-64. Public Key List Parameter Format

3.2.2.1.4.3.2.35 T2 (Link Retransmission Timer) (ID 42)

a) The bit format of the T2 parameter **shall**[283] be encoded/decoded as indicated in Figure 3-65.

	First bit Trans-mitted	Bit Number						
Octet	1	2	3	4	5	6	7	8
1	T2				0	0	0	0

- T2 field has a range of 1 to 10 with a step size of 1.

Figure 3-65. T2 Parameter Format

3.2.2.1.4.3.2.36 MDR ID Number (ID 50)

a) The bit format of the MDR ID Number parameter **shall**[12] be encoded/decoded as indicated in Figure 3-66.

	First bit Trans-mitted	Bit Number						
Octet	1	2	3	4	5	6	7	8
1								(msb)
2	MDR ID							
3	(lsb)							

- MDR ID is linearly encoded/decoded from 0 to 16777215.

Figure 3-66. MDR ID Number Parameter Format

3.2.2.1.4.3.2.37 RF Input Power Level (AM) (ID 51)

a) The bit format of the RF Input Power Level parameter **shall**[20] be encoded/decoded as indicated in Figure 3-67.

	First bit Trans-mitted	Bit Number						
Octet	1	2	3	4	5	6	7	8
1	RF Input Power Level Setting							0

- RF Input Power field is encoded as:
  Measured RF Input Power Level (dBm) + 110.
- Since the Measure RF Input Power Level has a range of -110 to +15 dBm, the RF Input Power field has a valid range of 0 to 125.

Figure 3-67. RF Input Power Level Parameter Format

3.2.2.1.4.3.2.38 Squelch Break Status (AM) (ID 52)

a) The bit format of the Squelch Break Status parameter **shall**[26] be encoded/decoded as indicated in Figure 3-68.

	First bit Trans-mitted	Bit Number						
Octet	1	2	3	4	5	6	7	8
1	Squelch Break							

- Where Squelch Break is encoded/decoded as follows:
  0 = Squelch Closed
  255 = Squelch Open

Figure 3-68. Squelch Break Status Parameter Format

3.2.2.1.4.3.2.39 In-Service Time (ID 53)

a) The bit format of the In-Service Time parameter **shall**[32] be encoded/decoded as indicated in Figure 3-69.

	First bit Trans-mitted	Bit Number						
Octet	1	2	3	4	5	6	7	8
1								(msb)
2	In-Service Time (Hours)							
3	(lsb)							

- In-Service Time is linearly encoded/decoded in steps of 1 hour.

Figure 3-69. In-Service Time Parameter Format

3.2.2.1.4.3.2.40 RIU Timing Offset Change (VDL Mode 3) (ID 54)

a) The bit format of the RIU Timing Offset Change parameter **shall**[50] be encoded/decoded as indicated in Figure 3-70.

	First bit Trans-mitted	Bit Number						
Octet	1	2	3	4	5	6	7	8
1	RIU Timing Status							

- Where RIU Timing Status is encoded/decoded as follows:
  0 = No Time Slip
  255 = Time Slip

Figure 3-70. RIU Timing Offset Change Parameter Format

3.2.2.1.4.3.2.41 Transmit Antenna VSWR (ID 55)

a) The bit format of the Transmit Antenna VSWR parameter **shall**[66] be encoded/decoded as indicated in Figure 3-71.

	First bit Trans-mitted	Bit Number						
Octet	1	2	3	4	5	6	7	8
1	VSWR							

- Where VSWR is encoded/decoded as follows:
  0 = Good
  255 = Bad

Figure 3-71. Transmit Antenna VSWR Parameter Format

3.2.2.1.4.3.2.42 RESERVED (ID 56)

3.2.2.1.4.3.2.43 Measured Power Output (ID 57)

a) The bit format of the Measured Power Output parameter **shall**[284] be encoded/decoded as indicated in Figure 3-72.

	First bit Trans-mitted	Bit Number						
Octet	1	2	3	4	5	6	7	8
1	Measured PowerOutput						0	0

- The Measured PowerOutput field is encoded as:
  Power Output measured at the MDR RF Output (in dBm)*2 - 60.
- Measured PowerOutput field has a range of 0 to 40, with 0 representing Power Output measured at the MDR antenna connector less than or equal to 30 dBm, and 40 representing Power Output measured at the MDR RF Output equal to or greater than 50 dBm.

Figure 3-72. Measured Power Output Parameter Format

3.2.2.1.4.3.2.44 Measured Transmitter Modulation % (ID 58)

a) The bit format of the Measured Transmitter Modulation % parameter **shall**[285] be encoded/decoded as indicated in Figure 3-73.

	First bit Trans-mitted	Bit Number						
Octet	1	2	3	4	5	6	7	8
1	Measured Modulation %							0

- Linearly encoded/decoded measured transmitter modulation % from 0 to 100 in steps of 1, as measured at the MDR RF Output.

Figure 3-73. Measured Transmitter Modulation % Parameter Format

3.2.2.1.4.3.3 RIU/MDR Status

The RIU/MDR Status message is used to send MDR status information from the MDR to the RIU every 240 milliseconds. The RIU/MDR Status message is also used to send the Link Initialization Sequence number from the RIU to the MDR, which completes the Link Initialization procedure as described in section 3.2.2.6.2.1. The general format of the RIU/MDR Status message is defined in section 3.2.2.6.5.1.8. This section defines the format of the 16-bit information payload field of the RIU/MDR Status Message for the MDR transmitters and the MDR receiver.

3.2.2.1.4.3.3.1 MDR Transmitter RIU/MDR Status Word

a) For the MDR transmitters, the RIU/MDR Status word **shall**[140] comprise the fields specified in Table 3-3.

Table 3-3. MDR Transmitter RIU/MDR Status Word Fields

Bit Ordering							
1 (lsb)	2	3	4	5	6	7	8 (msb)
Spare	*Spare*	F	I	T	S_1	S_2	S_3
Spare	*Spare*	*Spare*	*Spare*	*Spare*	D	V	M

3.2.2.1.4.3.3.1.1 Status (S)

a) The S bits indicate the operational status of the MDR component and **shall**[141] be encoded as follows:
   - 0 = Offline
   - 1 = Power Down (if exercised)
   - 2 = Power Up
   - 3 = Online
   - 4-5 = Reserved
   - 6 = Recovery
   - 7 = Fail.

3.2.2.1.4.3.3.1.2 RIU Timing Status (T)

a) The T bit **shall**[142] be encoded as follows:
   - 0 = MDR MAC cycle timing not locked to 6-second epoch
   - 1 = MDR MAC cycle timing locked to 6-second epoch.

3.2.2.1.4.3.3.1.3 Invalid RIU Data (I)

a) The I bit **shall**[143] be encoded as 1 if any invalid data was received from the RIU during the last MAC cycle, or 0 otherwise. Invalid data is associated with the HDLC formatting and the message headers defined in Section 3.2.2.6.5. Examples of invalid data are header fields out of range, unknown message ID, inappropriate HDLC frame type, and HDLC frame shorter than indicated frame length.

3.2.2.1.4.3.3.1.4 T1 Frame Slip (F)

a) The F bit **shall**[144] be encoded as 1 if a T1 Frame Slip was detected on the link from the RIU, or 0 otherwise.

3.2.2.1.4.3.3.1.5 Reserved

3.2.2.1.4.3.3.1.6 M-Channel Data Underflow (M)

a) The M bit **shall**[146] be encoded as 1 if any M-channel data within the last MAC cycle was not received from the RIU in time to be modulated, or 0 otherwise.

3.2.2.1.4.3.3.1.7 V-Channel Data Underflow (V)

a) The V bit **shall**[147] be encoded as 1 if any Voice Channel data within the last MAC cycle was not received from the RIU in time to be modulated, or 0 otherwise.

3.2.2.1.4.3.3.1.8 D-Channel Data Underflow (D)

a) The D bit **shall**[148] be encoded as 1 if any Data Channel data within the last MAC cycle was not received from the RIU in time to be modulated, or 0 otherwise.

3.2.2.1.4.3.3.2 MDR Receiver RIU/MDR Status Word

For the MDR receiver, the RIU/MDR Status word **shall**[149] comprise the fields specified in Table 3-4.

Table 3-4. MDR Receiver RIU/MDR Status Word Fields

Bit Ordering							
1 (lsb)	2	3	4	5	6	7	8 (msb)
Spare	*Spare*	F	I	T	S_1	S_2	S_3
Spare	*Spare*	*Spare*	*Spare*	*Spare*	*Spare*	*Spare*	*Spare*

3.2.2.1.4.3.3.2.1 Status (S)

a) The S bits indicate the operational status of the MDR component and **shall**[150] be encoded as follows:
   - 0 = Offline
   - 1 = Power Down (if exercised)
   - 2 = Power Up
   - 3 = Online
   - 4-5 = Reserved
   - 6 = Recovery
   - 7 = Fail.

3.2.2.1.4.3.3.2.2 RIU Timing Status (T)

a) The T bit **shall**[151] be encoded as follows:
   0 = MDR MAC cycle timing not locked to 6-second epoch
   1 = MDR MAC cycle timing locked to 6-second epoch.

3.2.2.1.4.3.3.2.3 Invalid RIU Data (I)

a) The I bit **shall**[152] be encoded as 1 if any invalid data was received from the RIU during the last MAC cycle, or 0 otherwise. Invalid data is associated with the HDLC formatting and the message headers defined in Section 3.2.2.6.5. Examples of invalid data are header fields out of range, unknown message ID, inappropriate HDLC frame type, and HDLC frame shorter than indicated frame length.

3.2.2.1.4.3.3.2.4 T1 Frame Slip (F)

a) The F bit **shall**[153] be encoded as 1 if a T1 Frame Slip was detected on the link from the RIU, or 0 otherwise.

3.2.2.1.4.3.3.2.5 Reserved

3.2.2.1.4.3.3.2.6 Reserved

3.2.2.2 Presentation Layer (NA)

3.2.2.3 Session Layer (NA)

3.2.2.4 Transport Layer (NA)

3.2.2.5 Network Layer (NA)

3.2.2.6 Data Link Layer

The Data Link Layer protocol for the MDR/RIU Interface is based on ISO/IEC 4335, the High-level Data Link Control (HDLC) Elements of Procedures. Outside of Link Initialization and Link Clearing, this link will operate as a balanced-operation connectionless-mode, per ISO/IEC 7809 HDLC Classes of Procedures, using Option 12 supporting the TEST frame. The following subsections define the characteristics of the Data Link Layer.

3.2.2.6.1 HDLC Frame Structure

The basic unit of transmission is the frame, which is a bit sequence containing at least 32 bits between flags (eight address, eight control, and 16 frame check sequence bits).
All non-segmented messages or individual message segments (of a segmented message) sent between the MDR and RIU **shall**[158] be transmitted within one frame. Transmissions conform to the HDLC frame structure shown in Figure 3-74, HDLC Frame Structure.

Flag Sequence	Address	Control	Information	Frame Check Sequence	Flag Sequence
01111110	8 bits	8 bits	Variable - messages	16 bits	01111110

Figure 3-74. HDLC Frame Structure

3.2.2.6.1.1 Flag Sequence Field

The Flag (F) Sequence field appears at the beginning and end of all frames and **shall**[159] consist of one 0 bit followed by six contiguous 1 bits and one 0 bit. The F field is used to mark the beginning and end of each frame. The F field at the end of the HDLC frame may serve as the start of the next HDLC frame.

3.2.2.6.1.2 Address Field

The Address (AD) field consists of one octet. For all HDLC messages except the TEST Response message, the AD field **shall**[160] contain the address of the unit **to** which the information sequence in the frame is sent. For TEST Response messages, the AD field **shall**[286] contain the address of the unit **from** which the information sequence in the frame is sent. The coding of the AD field is defined in ISO 3309.

3.2.2.6.1.2.1 RIU Address

a) The RIU will encode the HDLC address as 01 for all HDLC Test Response messages to be delivered to the MDR.

b) The MDR **shall**[287] encode the HDLC address as 01 for all HDLC UI messages to be delivered to the RIU.

c) The RIU will accept and process HDLC UI messages from the MDR with the HDLC address encoded as 01.

3.2.2.6.1.2.2 MDR Address

a) MDR transmitters **shall**[296] encode the HDLC address as 02 for all HDLC Test Response messages to be delivered to the RIU.

b) MDR receivers **shall**[297] encode the HDLC address as 03 for all HDLC Test Response messages to be delivered to the RIU.The RIU will accept and process HDLC Test Response messages from MDR transmitters with the HDLC address encoded as 02.

d) The RIU will accept and process HDLC Test Response messages from MDR receivers with the HDLC address encoded as 03.

e) MDR transmitters **shall**[298] accept and process HDLC UI messages from the RIU with the HDLC address encoded as 02.

f) MDR receivers **shall**[299] accept and process HDLC UI messages from the RIU with HDLC address encoded as 03.

3.2.2.6.1.3 Control Field

The Control (CN) field consists of one octet and **shall**[161] be used to identify the frame type, either TEST or Unnumbered Information (UI). A TEST frame may be either a TEST Command or TEST Response. All Unnumbered Information (UI) frames **shall**[290] be UI Command frames. The Poll/Final bit (bit 5) in the Control Field is not used and **shall**[291] be set to 0. The content of the Control field is defined in ISO 4335.

3.2.2.6.1.4 Information Field

The Information (I) field of a frame follows the CN field and precedes the Frame Check Sequence. Information may be in any sequence of bits. In a UI frame, the I field **shall**[162] contain a message. These messages are defined in section 3.2.2.6.5.1, General Message Structure. The I field **shall**[163] consist of an integral number of octets.

3.2.2.6.1.5 Frame Check Sequence Field

The Frame Check Sequence (FCS) field **shall**[164] consist of 16 bits and be used for frame error detection. The FCS field is defined in ISO 3309.

3.2.2.6.1.6 Inter Frame Time Fill

The time between frames **shall**[300] be filled with flag characters, per ISO 3309.

3.2.2.6.2 Link Control Functions

The state of the link is determined by the Link Control functions, which are defined in the following subsections: Link Initialization; Link Maintenance; Link Clearing; and Link Exception Reporting. These Link Control functions are consistent with the link parameters defined in section 3.2.2.6.3, Link Level Parameters.

3.2.2.6.2.1 Link Initialization

The MDR and RIU will work in either one of two states. These two states of operation **shall**[165] be defined as the *link inactive* state and *link initialized* state. By default, the MDR and RIU will both start in the *link inactive* state.
The RIU will initiate the Link Initialization procedure. The Link Initialization procedure **shall**[166] consist of the RIU generating a Test Command to the MDR with a four-octet (octet 1 is MSB, octet 4 is LSB) I field consisting of a sequence number starting at zero and incrementing by one with each retransmission.
Upon receipt of the TEST Command, the MDR will issue a TEST Response echoing the I field received in the TEST Command. If the RIU receives a valid TEST Response (one

containing a matching I field) within the T1 setting, the RIU will consider itself in the *link initialized* state, cancel the T1 timer, and issue a RIU/MDR Status message. Upon receipt of the RIU/MDR Status message, the MDR will consider itself in the *link initialized* state. A nominal case of Link Initialization is illustrated in Figure 3-75a.

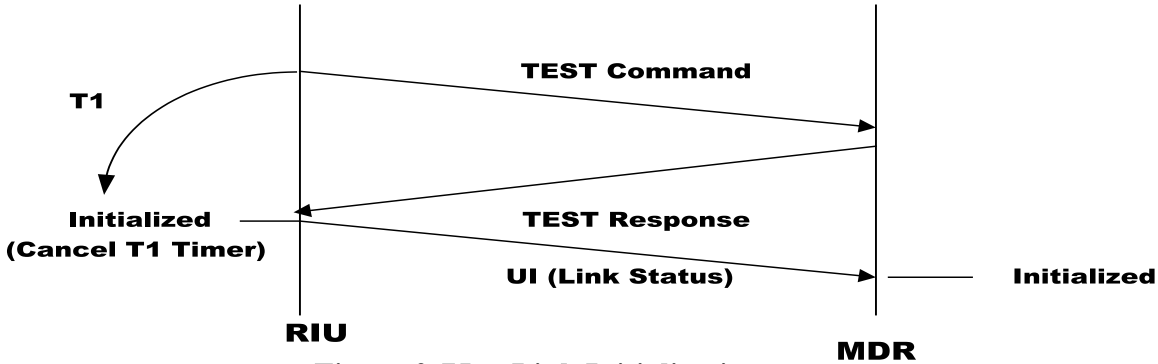


Figure 3-75a. Link Initialization

Otherwise, in the event the T1 Timer expires the RIU will continuously send the TEST Command based on expiration of the T2 Link Retransmission Timer.

If the RIU receives the TEST Response from the MDR outside the T1 timer, the response is discarded, and the RIU will retransmit the TEST Command upon expiration of the T2 timer.

3.2.2.6.2.2 Link Maintenance

Once in the *link initialized* state, the Link Maintenance procedure occurs. The Link Maintenance procedure will consist of the MDR sending a RIU/MDR Status messages to the RIU every 240 ms.

3.2.2.6.2.3 Link Clearing

Either the MDR or RIU may clear the link at any time. While in the *link initialized* state, the initiator of the Link Clearing procedure **shall**[168] send a TEST Command message with a five-octet information field, the first four octets (octet 1 is MSB, octet 4 is LSB) containing all ONEs indicating a clear, followed by a one octet clearing cause code. Clearing Cause codes are represented in Table 3-5.

Table 3-5. Coding of the Clearing Cause Field

Clearing Cause	Bit Ordering							
	1(lsb)	2	3	4	5	6	7	8(msb)
RIU Originated	0	0	0	0	0	0	0	0
MDR Originated	1	1	1	1	1	1	1	1

Note: The MDR vendor may supplement the Clearing Cause table as they deem appropriate using values of 128 - 254.

The recipient of the line clearing procedure **shall**[169] confirm the clear by issuing a TEST Response with the first four octets set to all ONEs. Upon receipt of a valid TEST Response confirming the clear, the initiator **shall**[257] clear the T1 timer, and both the MDR and RIU will be in the *link inactive* state.

In the event the T1 Timer expires, the initiator of the clear will continuously send the clearing TEST Command based on expiration of the T2 Link Retransmission Timer, until a valid TEST response is received clearing the link, which will set the initiator of the clear into the *link inactive* state.

If the initiator of the clear receives the TEST Response from the recipient outside the T1 timer, the response is discarded, and the initiator will retransmit the TEST Command upon expiration of the T2 timer.

The nominal Link Clearing threads are illustrated in Figure 3-75b, and 3-75c.

If a TEST Command is received that indicates "link clearing", while in the link inactive state, a TEST Response will be generated closing the link. This case may occur if a TEST Response message was lost in transmission.

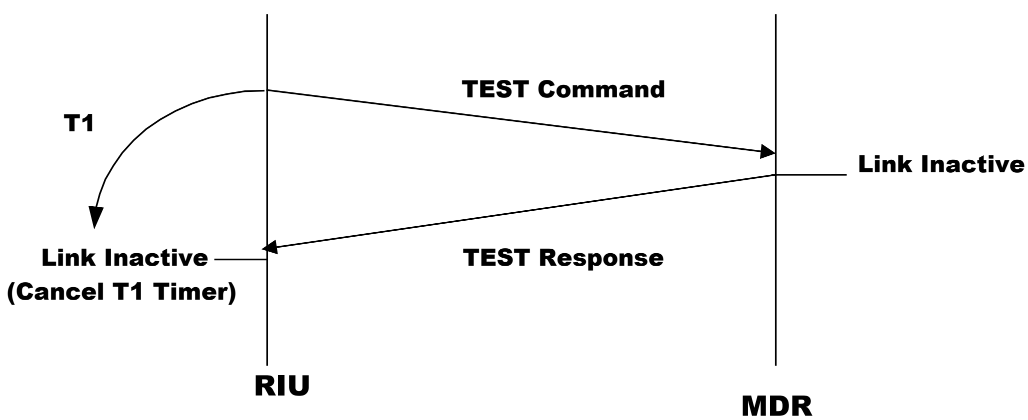


Figure 3-75b. RIU Initiated Link Clearing

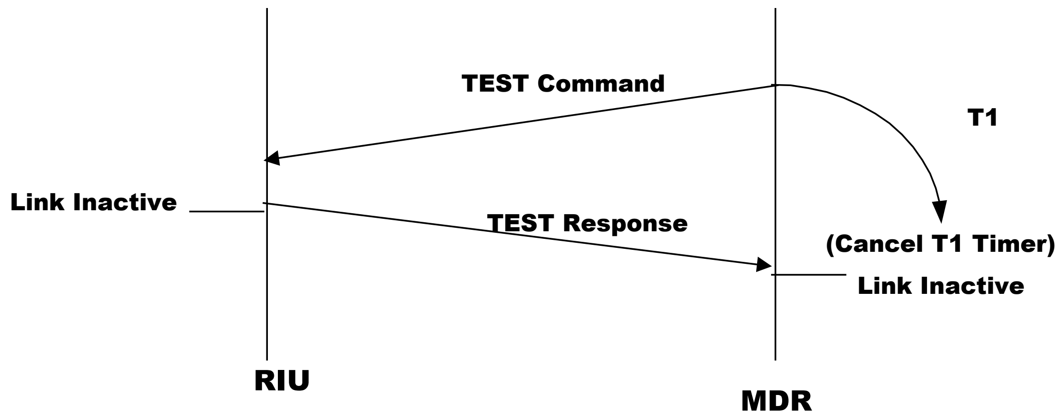


Figure 3-75c. MDR Initiated Link Clearing

3.2.2.6.2.4 Link Exception Reporting

If the RIU does not detect the RIU/MDR Status message for N2 successive times, it will notify the RMMC function that the applicable MDR is considered failed. The RIU will enter the *link inactive* state and reattempt link initialization per section 3.2.2.6.2.1, Link Initialization.

3.2.2.6.3 Link Level Parameters

The MDR/RIU Interface Link Level Parameters are defined in accordance with Table 3-6.

Table 3-6. Link Level Parameters

Parameter	Description	Min	Max	Default
N1	Maximum number of information field bits	128	4096	512
N2	Link Status Counter	1	64	12
T1	Link response timer	100 ms	500 ms	200 ms
T2	Link retransmission timer	1 sec	10 sec	5 sec
T3	Reassembly Timer	50 ms	65,535 ms	250 ms

3.2.2.6.4 HDLC Frame Timing

The timing and size of HDLC frame transmissions between the MDR and RIU **shall**[171] be controlled such that the voice delay from start of first bit at the originator (MDR/RIU) to the reception of the last bit at the recipient (RIU/MDR), due to HDLC frame transmission, does not exceed 3 ms. The MDR and RIU will order frames for transmission to ensure that Voice messages reach their destination no more than 5.18 ms before they are required and no later than when they are required. To meet these requirements in VDL modes that require voice operation, the N1 parameter must not exceed 512. These requirements do not apply for PCM voice operation.

Note 1: These requirements are levied upon the transmission device to ensure appropriate prioritization of the messages as well as the appropriate prioritization of the software tasks.
Note 2: The 5.18 ms requirement provides time for a different maximum size (N1 fully bit-stuffed) burst to complete transmission and then for the necessary Voice message to be transmitted across the link, assuming the necessary message is needed just-in-time. For example, the required point for the RIU transmission of the last Voice Burst message segment (VFSN = 6 in message header) is to get the message to the MDR transmitter at most 6 ms before the time required to begin modulation of the 6^{th} vocoder frame. The required point for the MDR receiver transmission of the first vocoder frame (VFSN = 1) in a voice reception is to get the message to the RIU at most T_{RXV1} seconds after the start of the VDL Mode 3 6-second epoch in which the burst was received (T_{RXV1} is defined in Appendix D).

3.2.2.6.5 Link Level Message Description

A message is contained within an I field of a UI frame. Each message exchanged across the data interface **shall**[172] contain a one octet Message ID followed by the message. The UI frame and its components are illustrated in Figure 3-76, Link Level Message Structure.

Flag Sequence	Address	Control	Information	FCS	Flag Sequence

Message ID	Message

Figure 3-76. Link Level Message Structure

3.2.2.6.5.1 General Message Structure

The general message structure is comprised of the Message ID and Message Type. The Message ID values and Message Type identifiers are defined in Table 3-7, Message Transmission Capability. This table also defines the transmission source associated with each Message Type for the RIU-MDR Transmitter and RIU-MDR Receiver links.

The message format diagrams (Figures 3-77 through 3-83) in the remainder of this section specify bit 1 of each octet as the first bit transmitted. Note that bit 1 of each octet is the first bit of the octet transmitted over the T1 Data Channel as specified in section 3.2.2.7.1.3.3.d. Bit 1 of each octet is also the lsb of the octet. Due to HDLC zero-bit insertion, message octets are not necessarily aligned on T1 time slot boundaries.

Unless otherwise specified in the remainder of this section, bit fields **shall**[258] be encoded such that the most significant bit of a field (or sub-field that crosses octet boundaries) is in the highest bit number position of the octet.

For variable length bit fields that have a total length (LEN) that is not a multiple of 8, the most significant bit of the part-octet (remaining part of the field) at the end of the field **shall**[259] be encoded in bit 8 of the last octet and the unused lower numbered bit(s) in the last octet **shall**[260] be set to 0.

Table 3-7. Message Transmission Capability

Message ID	Message Type	RIU-Transmitter Link		RIU-Receiver link	
		RIU	MDR	RIU	MDR
0	Voice-Burst	X			X
1	Data-Burst	X			X
2	Management-Burst	X			X
3	Sync Search Control			X	
4	PCM Voice	X			X
5	Radio Control	X	X	X	X
6	Radio Monitoring		X		X
7	RIU/MDR Status	X	X	X	X
8-255	Reserved				

3.2.2.6.5.1.1 Voice-Burst Message

The Voice-Burst message will be transmitted between the MDR and the RIU and contains a message ID of 0. The Voice-Burst message **shall**[176] be encoded as illustrated in Figure 3-77 with the field descriptions shown in Table 3-8. The Vocoder Frame Sequence Number (VFSN) indicates which 96-bit vocoder frame (1-6) contained within the TDMA time slot is the starting frame of the enclosed information in the VF field. For example, if the Voice-Burst contains the second and third vocoder frames, the VFSN field would indicate 2 and the LEN field would indicate 192. Segmentation is performed to minimize VDL Mode 3 voice delay. The TOA/TOT field **shall**[261] be the same value for all Voice-Burst message segments related to the same VDL Mode 3 voice burst. VDL Mode 3 voice burst D8PSK symbols **shall**[262] be mapped to Voice-Burst message VF octets as specified in Table 3-8a. Requirements for Voice-Burst message timing, exception handling, and rules for grouping vocoder frames within Voice-Burst messages are different for the RIU and MDR, and are defined in FAA-E-2938.

<table>
<tr><td></td><td>First bit Trans-mitted</td><td colspan="7">Bit Number</td></tr>
<tr><td>Octet</td><td>1</td><td>2</td><td>3</td><td>4</td><td>5</td><td>6</td><td>7</td><td>8</td></tr>
<tr><td>1</td><td colspan="8">VH (msb)</td></tr>
<tr><td>2</td><td colspan="4">(lsb) VH</td><td colspan="3">(lsb) VFSN</td><td>Spare</td></tr>
<tr><td>3</td><td colspan="8">LEN (msb)</td></tr>
<tr><td>4</td><td colspan="4">(lsb) LEN</td><td colspan="4">TOA/TOT (msb)</td></tr>
<tr><td>5</td><td colspan="8">TOA/TOT</td></tr>
<tr><td>6</td><td colspan="8">(lsb) TOA/TOT</td></tr>
<tr><td>7</td><td colspan="3">(lsb) GEC (msb)</td><td colspan="5">Spare</td></tr>
<tr><td>8</td><td colspan="8">(lsb) PWR (msb)</td></tr>
<tr><td>9+</td><td colspan="8">VF (variable)</td></tr>
</table>

Figure 3-77. Voice-Burst Message Format

Table 3-8. Voice-Burst Field Description

Field	Field Length (bits)	Description
VH[1]	12	Voice Header derived from the RIU, for MDR transmitters, or from the aircraft transmitter, for MDR receivers. See RTCA DO-224a for more details.
VFSN	3	Vocoder Frame Sequence Number (1-6)
Spare	1	Spare (Set field = 0)
LEN	12	Length of VF field (bits)
TOA/TOT[1]	20	Time of Arrival (receiver-to-RIU) Time of Transmission (RIU-to-transmitter) Range: 0 to 1,007,999, 1/16th D8PSK symbol resolution See section 3.2.2.7.2.
GEC	3	Header Golay Error Count (0 - 3, 4 uncorrectable – Rx to RIU) (0, RIU to TX)
Spare	5	Spare (Set field = 0)
PWR[1]	8	Power Output (33 – 47dBm in 0.5dB steps) for RIU-to-TX. PWR = (Power*2 - 60) which yields PWR = 6 for 33dBm and PWR = 34 for 47dBm. Received Power (-110 – +15dBm in 0.5dBm steps) for Rx-to-RIU. PWR = 0 for –110dBm and PWR = 250 for +15dBm
VF	LEN	Vocoder Field Data: Bit format defined in Table 3-8a

Note 1: These fields (VH, TOA/TOT, PWR) will contain the same value for all Voice-Burst message segments related to the same VDL Mode 3 voice burst.

Table 3-8a. Voice-Burst VF field and Data-Burst DF field Description

D8PSK Symbol No. within 96-bit Voice Frame N or Data Segment N	D8PSK Symbol Most Significant Bit		D8PSK Symbol Least Significant Bit	
	V/D Message Octet No.	Bit No. in Octet	V/D Message Octet No.	Bit No. in Octet
1	12*(N-1)+9	8	12*(N-1)+9	6
2	12*(N-1)+9	5	12*(N-1)+9	3
3	12*(N-1)+9	2	12*(N-1)+10	8
4	12*(N-1)+10	7	12*(N-1)+10	5
5	12*(N-1)+10	4	12*(N-1)+10	2
6	12*(N-1)+10	1	12*(N-1)+11	7
7	12*(N-1)+11	6	12*(N-1)+11	4
8	12*(N-1)+11	3	12*(N-1)+11	1
9	12*(N-1)+12	8	12*(N-1)+12	6
10	12*(N-1)+12	5	12*(N-1)+12	3
11	12*(N-1)+12	2	12*(N-1)+13	8
12	12*(N-1)+13	7	12*(N-1)+13	5
13	12*(N-1)+13	4	12*(N-1)+13	2
14	12*(N-1)+13	1	12*(N-1)+14	7
15	12*(N-1)+14	6	12*(N-1)+14	4
16	12*(N-1)+14	3	12*(N-1)+14	1
17	12*(N-1)+15	8	12*(N-1)+15	6
18	12*(N-1)+15	5	12*(N-1)+15	3
19	12*(N-1)+15	2	12*(N-1)+16	8
20	12*(N-1)+16	7	12*(N-1)+16	5
21	12*(N-1)+16	4	12*(N-1)+16	2
22	12*(N-1)+16	1	12*(N-1)+17	7
23	12*(N-1)+17	6	12*(N-1)+17	4
24	12*(N-1)+17	3	12*(N-1)+17	1
25	12*(N-1)+18	8	12*(N-1)+18	6
26	12*(N-1)+18	5	12*(N-1)+18	3
27	12*(N-1)+18	2	12*(N-1)+19	8
28	12*(N-1)+19	7	12*(N-1)+19	5
29	12*(N-1)+19	4	12*(N-1)+19	2
30	12*(N-1)+19	1	12*(N-1)+20	7
31	12*(N-1)+20	6	12*(N-1)+20	4
32	12*(N-1)+20	3	12*(N-1)+20	1

Notes:

1) N = 1 for the first Vocoder Frame Segment in a Voice-Burst message and for the first Data Segment in a Data-Burst message. N = 1 to (LEN/96).

2) For each voice/data segment, D8PSK symbol No. 1 is the first VDL Mode 3 symbol transmitted/received and D8PSK symbol No. 32 is the last VDL Mode 3 symbol transmitted/received.

3.2.2.6.5.1.2 Data-Burst Message

The Data-Burst message will be transmitted between the MDR and the RIU and contains a message ID of 1. The Data-Burst message **shall**[178] be encoded as illustrated in Figure 3-78 with the field descriptions shown in Table 3-9. The Data-Burst message is segmented across the MDR and RIU interface. Segmentation is performed so that time critical messages such as voice are not delayed across the interface. The Data Segment Number (DSN) indicates which 96-bit data segment (1-6) contained within the TDMA time slot is the starting segment of the enclosed information in the DF field. For example, if the Data-Burst message contains the fourth, fifth and sixth data segments, the DSN field would indicate 4 and the LEN field would indicate 288. A message is deemed valid by the receiver, if all six data segments are received in sequence prior to the expiration of the T3 timer. If any segment is received out of order, or the T3 timer expires prior to the receipt of all segments corresponding to the TOA/TOT field, all segments are discarded. The VDL Mode 3 Link Layer will provide for retransmission of the lost data. The TOA/TOT field **shall**[263] be the same value for all Data-Burst message segments related to the same VDL Mode 3 data burst. VDL Mode 3 data burst D8PSK symbols **shall**[264] be mapped to Data-Burst message DF octets as specified in Table 3-8a.

	First bit Trans-mitted	Bit Number						
Octet	1	2	3	4	5	6	7	8
1					DH			(msb)
2	(lsb)	DH			(lsb)	DSN	(msb)	Spare
3					LEN			(msb)
4	(lsb)	LEN				TOA/TOT		(msb)
5					TOA/TOT			
6	(lsb)				TOA/TOT			
7	(lsb)	GEC	(msb)			Spare		
8	(lsb)				PWR			(msb)
9+					DF (variable)			

Figure 3-78. Data-Burst Message Format

Table 3-9. Data-Burst Field Description

Field	Field Length (bits)	Description
DH	12	Data Header derived from the RIU, for MDR transmitters, or from the aircraft transmitter, for MDR receivers. See RTCA DO-224a for more details.
DSN	3	Data Segment Number: DF field of message starts with DSN (1-6). Each segment contains 96-bits of data.
Spare	1	Spare (Set field = 0)
LEN	12	Length of DF field (bits). Max. size = 384 bits. LEN is a multiple of 96.
TOA/TOT	20	Time of Arrival (receiver-to-RIU) Time of Transmission (RIU-to-transmitter) Range: 0 to 1,007,999, 1/16th D8PSK symbol resolution See section 3.2.2.7.2.
GEC	3	Header Golay Error Count (0 - 3, 4 uncorrectable – Rx to RIU) (0, RIU to TX)
Spare	5	Spare (Set field = 0)
PWR	8	Power Output. See PWR field, Table 3-8
DF	LEN	R-S Coded Data: Bit format defined in Table 3-8a

3.2.2.6.5.1.3 Management-Burst Message

The Management-Burst message will be transmitted between the MDR and the RIU and contains a message ID of 2. The Management-Burst message **shall**[180] be encoded as illustrated in Figure 3-79 with the field descriptions shown in Table 3-10. The Management-Burst message is not segmented across the MDR to RIU interface.

The Synchronization Header Type (STYPE) field **shall**[183] be encoded per Table 3-10a. This field identifies which synchronization sequence is to be used per the VDL Mode 3 RTCA DO-224a.

The MB field **shall**[265] be encoded with the most significant bit of each VDL Mode 3 12-bit Management Burst word placed in the highest unused bit number position in the octet. As Management Burst words cross octet boundaries, the most significant bit of the remaining 12-bit Management Burst word **shall**[266] be placed in bit 8 of the next octet. For example, the most significant bit of the first 12-bit Management Burst word in the message resides in bit 8 of octet 9. The most significant bit of the second 12-bit Management Burst word begins in bit 4 of octet 10, and so forth.

	First bit Transmitted	Bit Number						
Octet	1	2	3	4	5	6	7	8
1	(lsb) STYPE		Spare					
2	Spare							
3	LEN (msb)							
4	(lsb) LEN				TOA/TOT (msb)			
5	TOA/TOT							
6	(lsb) TOA/TOT							
7	(lsb) GEC1 (msb)			Spare	(lsb) GEC2 (msb)			Spare
8	(lsb) PWR (msb)							
9+	MB (variable)							

Figure 3-79. Management-Burst Message Format

Table 3-10. Management -Burst Field Description

Field	Field Length (bits)	Description
STYPE	2	Sync Header Type (See Table 3-10a)
Spare	14	Spare (Set field = 0)
LEN	12	Length of Segment = MB field in bits
TOA/TOT	20	Time of Arrival (receiver-to-RIU) Time of Transmission (RIU-to-transmitter) Range: 0 to 1,007,999, 1/16th D8PSK symbol resolution See section 3.2.2.7.2.
GEC1	3	Golay Word1 Error Count (0-3, 4 uncorrectable – Rx to RIU) (0, RIU to TX)
Spare	1	Spare (Set field = 0)
GEC2	3	Golay Word2 Error Count (0-3, 4 uncorrectable – Rx to RIU) (0, RIU to TX)
Spare	1	Spare (Set field = 0)
PWR	8	Power Output. See PWR field, Table 3-8
MB	LEN	Management-Burst words

Table 3-10a. STYPE Field Description

STYPE	Synchronization Sequence
0	S_1 and S_1*
1	Reserved
2	S_2
3	S_2*

3.2.2.6.5.1.4 Sync Search Control Message

The Sync Search Control message will be transmitted from the RIU to the MDR receiver and contains a message ID of 3. The Sync Search Control message **shall**[186] be encoded as illustrated in Figure 3-80 with the field descriptions shown in Table 3-11. The Sync Search Control message is not segmented across the RIU to MDR interface. The Synchronization Header Type (STYPE) field **shall**[267] be encoded per Table 3-10a. This field identifies which synchronization sequence(s) the MDR receiver must search for per FAA-E-2938. When STYPE is specified as 0, the MDR receiver is required to search for both the S_1 and S_1* synchronization sequences at the same time. The synchronization sequences S_1, S_1*, S_2 and S_2* are defined in the VDL Mode 3 RTCA DO-224a. The NGW field **shall**[268] indicate the number of (24,12) Golay words in the received burst to be decoded by the MDR if synchronization is achieved within the search window. Although only two bits are presently required for the NGW field, five bits are provided for future expansion or to allow the RIU to monitor ground radio transmissions (e.g. 3T-management uplink burst).

The S_START and S_STOP fields define the Sync Search start and stop times, respectively, for the time window in the 6-second VDL Mode 3 epoch where the MDR receiver will search for a VDL Mode 3 synchronization signal as defined in section 3.2.2.7.2. The S_START and S_STOP fields specify the time window within the 6-second epoch where the center of the first D8PSK synchronization symbol must appear for the MDR receiver to declare sync.

<table>
<tr><td></td><td>First bit Trans- mitted</td><td colspan="7">Bit Number</td></tr>
<tr><td>Octet</td><td>1</td><td>2</td><td>3</td><td>4</td><td>5</td><td>6</td><td>7</td><td>8</td></tr>
<tr><td>1</td><td colspan="2">(lsb) STYPE</td><td colspan="5">(lsb) NGW (msb)</td><td>Spare</td></tr>
<tr><td>2</td><td colspan="8">S_START (msb)</td></tr>
<tr><td>3</td><td colspan="8">S_START</td></tr>
<tr><td>4</td><td colspan="4">(lsb) S_START</td><td colspan="4">S_STOP (msb)</td></tr>
<tr><td>5</td><td colspan="8">S_STOP</td></tr>
<tr><td>6</td><td colspan="8">(lsb) S_STOP</td></tr>
</table>

Figure 3-80. Sync Search Control Message Format

Table 3-11. Sync Search Control Field Description

Field	Field Length (bits)	Description
STYPE	2	Sync Header Type (See Table 3-10a)
NGW	5	Number of (24,12) Golay words to be demodulated by the MDR receiver. Range = 1 to 16.
Spare	1	Spare (Set field = 0)
S_START	20	Start of sync search window within 6-second epoch Range: 0 to 1,007,999, 1/16th D8PSK symbol resolution See Section 3.2.2.7.2
S_STOP	20	End of sync search window within 6-second epoch Range: 0 to 1,007,999, 1/16th D8PSK symbol resolution See Section 3.2.2.7.2

3.2.2.6.5.1.5 PCM-Voice Message

The PCM-Voice message will be sent via the link when operating in DSB-AM mode. The PCM Voice message will be transmitted between the MDR and RIU and contains a message ID of 4. The PCM Voice message **shall**[191] be encoded as illustrated in Figure 3-81 with the field descriptions shown in Table 3-12.

	First bit Trans-mitted	Bit Number						
Octet	1	2	3	4	5	6	7	8
1	EOM	Spare						
2	Spare							
3	LEN (msb)							
4	(lsb) LEN				TOA/TOT (N/A - set to 0)			
5	TOA/TOT (N/A - set to 0)							
6	TOA/TOT (N/A - set to 0)							
7	Spare							
8	(lsb) PWR (msb)							
9	First 16-bit PV word (msb)							
10	(lsb) First 16-bit PV word							
11+	Additional PV words							

Figure 3-81. PCM Voice Message Format

Table 3-12. PCM Voice Message Field Description

Field	Field Length (bits)	Description
EOM	1	End of Message flag (1 = last PCM message)
Spare	15	Spare (Set field = 0)
LEN	12	Length of PCM Voice data in bits (range: 16 to 3,200)
TOA/TOT	20	Not used, Set TOA/TOT field = 0
Spare	8	Spare (Set field = 0)
PWR	8	Power Output. See PWR field, Table 3-8
PV	LEN	PCM Voice words. 16-bit 2's complement format, MSB octet first, Bit 8 of MSB octet is the most significant bit of PCM word.

3.2.2.6.5.1.6 Radio Control Message

The Radio Control message provides a mechanism for transmission and reception of control information across the MDR to RIU interface. The Radio Control message will be transmitted between the MDR and the RIU and contains a message ID of 5. The Radio Control message **shall**[193] be encoded as illustrated in Figure 3-82 with the field descriptions shown in Table 3-13. The Radio Control message **shall**[194] be segmented across the interface if the message exceeds the segmentation size, defined by the N1 parameter. The Total Segment Count (TSC) field **shall**[195] indicate one less than the total number of segments for a specific transaction (identified by the TID field). For example, the TSC field is encoded as 4 when the total number of segments is 5. The Segment Count (SC) field **shall**[196] indicate the individual segment number for the transaction. A message **shall**[197] be deemed valid by the receiving unit, if all segments are received in sequence prior to the expiration of the T3 timer. If any segment is received out of order, or the T3 timer expires prior to the receipt of all segments corresponding to the TID field, all segments are discarded. It is the responsibility of the application to retransmit any lost data.

The Radio Control messages use a Request/Reply protocol. The MDR will respond to Control Request (RR = 1) messages with a Control Reply (RR = 0) message indicating whether or not the request is processed or fulfilling the request. Once the final segment of a Control Request (RR = 1) message is sent to the MDR, the RIU initiates a Reply response timer. The Reply Response timer is cancelled and the transaction is completed upon receipt of a control reply (RR = 0) from the MDR with a CTYPE and TID that match the request generated by the RIU. If the Reply Response timer expires, then the transaction is considered incomplete and the RIU will retransmit the request. If the MDR detects an error, it **shall**[292] be reported back in the reply by setting the ER field to 1, and placing the error cause code in the first octet of the message (MSG) field. The second and higher octets may be used to carry additional error information.
NOTE: The RIU will finish sending all segments associated with one control message before initiating another control message.

<table>
<tr><td></td><td>First bit Trans-mitted</td><td colspan="7">Bit Number</td></tr>
<tr><td>Octet</td><td>1</td><td>2</td><td>3</td><td>4</td><td>5</td><td>6</td><td>7</td><td>8</td></tr>
<tr><td>1</td><td colspan="8">(lsb) CTYPE (msb)</td></tr>
<tr><td>2</td><td>RR</td><td>ER</td><td colspan="2">PID</td><td colspan="4">(lsb) TSC (msb)</td></tr>
<tr><td>3</td><td colspan="4">(lsb) SC (msb)</td><td colspan="4">LEN (msb)</td></tr>
<tr><td>4</td><td colspan="8">(lsb) LEN</td></tr>
<tr><td>5</td><td colspan="2">(lsb) PRI (msb)</td><td colspan="6">TID (msb)</td></tr>
<tr><td>6</td><td colspan="8">(lsb) TID</td></tr>
<tr><td>7+</td><td colspan="8">MSG</td></tr>
</table>

Figure 3-82. Radio Control/Monitoring Message Format

Table 3-13. Radio Control/Monitoring Message Field Description

Field	Field Length (bits)	Description
CTYPE	8	Control Type – defines type of Control/Monitoring Message
RR	1	Request = 1, Reply = 0
ER	1	Error indication on reply only: ER = 0 - No error ER = 1 - Error on reply
PID	2	Protocol Identifier per Table 3-14a
TSC	4	Total Segment Count - Identifies the Total Segment Count of 1 - 16 segments (encoded as 0 - 15).
SC	4	Segment Count – Identifies the segment Modulo 16
LEN	12	Segment Length (bits)
PRI	2	Priority: Normal = 0, Alert = 1, Alarm = 2, Reserved = 3
TID	14	Transaction Identifier – Used to uniquely identify transactions Valid range of TID (1 – 16,383) 0 – Used by the MDR for unsolicited monitoring messages reply.
MSG	LEN	Control/Monitoring Message

Notes:

1) The format of the Control and Monitoring messages are defined in subsections of 3.2.2.1.4.3.1. and 3.2.2.1.4.3.2.
2) The CTYPE field corresponds to the ID number of parameters listed in Table 3-1.
3) If ER = 1, the MSG field contains the error code(s) defined in Table 3-14b.

Table 3-14a. Protocol Identifier (PID) Field Description

PID	Protocol
0	MDR Specific
1-3	Reserved

Table 3-14b. Error Codes

Error Code	Definition	User Data
0	RESERVED	N/A
1	Invalid Authentication	Attempted User ID(s), MDT# or REMOTE
2	Illegal Parameter ID	Unknown Parameter received
3	Parameter Out of Range	Illegal control parameter requested
4	Parameter Not Allowed	Parameter attempted
5	Upload Blocks Corrupted	TID
6-255	RESERVED	N/A

3.2.2.6.5.1.7 Radio Monitoring Message

The Radio Monitoring message provides a mechanism for transmission and reception of management information across the MDR to RIU interface. The Radio Monitoring message will be transmitted between the MDR and the RIU and contains a message ID of 6. The Radio Monitoring message **shall**[200] be encoded as illustrated in Figure 3-82 with the field descriptions shown in Table 3-13. The Radio Monitoring message **shall**[201] be segmented across the interface if the message exceeds the segmentation parameter, as defined by the N1 parameter. The TSC field **shall**[202] indicate one less than the total number of segments for a specific transaction (identified by the TID field). For example, the TSC field is encoded as 4 when the total number of segments is 5. The SC field **shall**[203] indicate the individual segment number for the current transaction. A message **shall**[204] be deemed valid by the receiver, if all segments are received in sequence prior to the expiration of the T3 timer. If any segment is received out of order, or the T3 timer expires prior to the receipt of all segments corresponding to the TID field, all segments are discarded. It is the responsibility of the application to retransmit any lost data.

Monitoring messages generated by the MDR as a result of an Alert or Alarm threshold crossing, **shall**[205] set the RR and TID fields to 0. The RIU does not respond to these messages.

3.2.2.6.5.1.8 RIU/MDR Status Message

The RIU/MDR Status message will define the status of the MDR or be used by the RIU to complete the link initialization. The RIU/MDR Status message will be transmitted between the MDR and RIU and contains a message ID of 7. The RIU/MDR Status message **shall**[208] be encoded as illustrated in Figure 3-83 with the field descriptions shown in Table 3-15. There is no segmentation of the RIU/MDR Status message.

	First bit Trans-mitted	Bit Number						
Octet	1	2	3	4	5	6	7	8
1	STATUS (msb)							
2	(lsb)							

Figure 3-83. RIU/MDR Status Message Format

Table 3-15. RIU/MDR Status Field Description

Field	Field Length (bits)	Description
Status	16	When sent by MDR: Bit fields defined in section 3.2.2.1.4.3.3. When sent by RIU: Value of "1" indicates link active.

3.2.2.7 Physical Layer

The MDR/RIU interface **shall**[209] implement the fractional T1 protocol as defined in ANSI T1.403-1995.

3.2.2.7.1 General Fractional T1 Characteristics

The following subparagraphs define the general characteristics of the physical interface used between the MDR and the RIU.

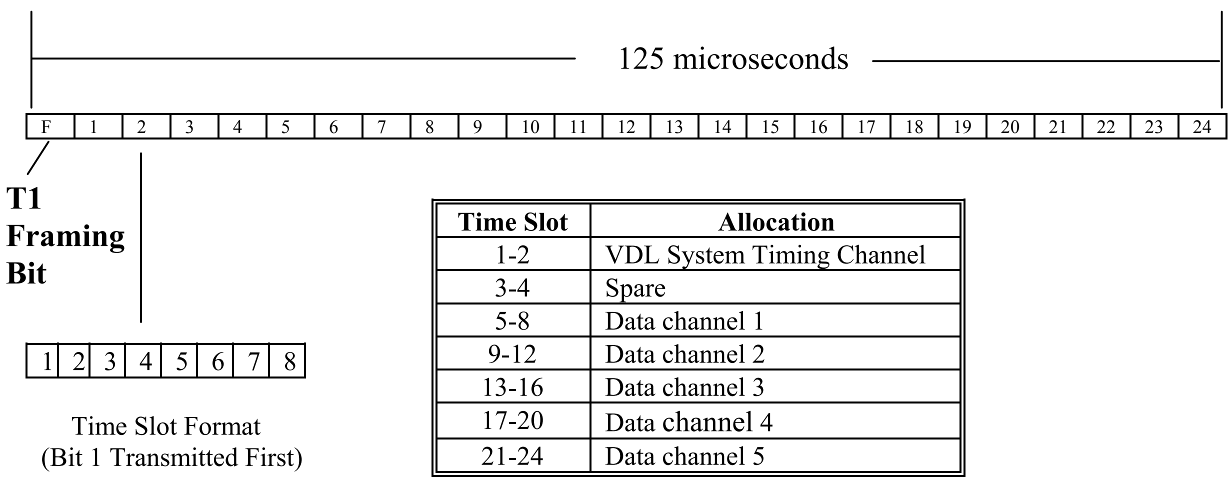
3.2.2.7.1.1 T1 Frame Characteristics

a) The following describes the basic characteristics for an MDR/RIU T1 line:
A T1 frame **shall**[210] consist of 193 bits.

b) Each T1 frame **shall**[211] be composed of one framing bit and twenty-four 8-bit time slots that carry data.

c) The framing bit **shall**[212] be the first bit of each frame.

d) The twenty-four 8-bit slots **shall**[213] be organized as described in Figure 3-84, T1 System Timing.



Time Slot	Allocation
1-2	VDL System Timing Channel
3-4	Spare
5-8	Data channel 1
9-12	Data channel 2
13-16	Data channel 3
17-20	Data channel 4
21-24	Data channel 5

Figure 3-84. T1 System Timing

e) The T1 line **shall**[214] transmit at a rate of 8,000 T1 frames/s, resulting in a bit rate of 1.544 Mbit/s.

f) The T1 line **shall**[215] use Extended Super Frame (ESF) formatting consisting of groups of 24 consecutive T1 frames.

g) The eighth bit of every time-slot in every sixth T1 frame **shall**[216] be used for data. In other words, robbed bit signaling is not to be used.

h) The ESF data link **shall**[217] support the Line Loopback Activate/Deactivate and Payload Loopback Activate/Deactivate messages to support line diagnostics and maintenance.

i) Pulse density **shall**[218] be accomplished using the Bipolar 8-Zero Substitution (B8ZS) method.

3.2.2.7.1.2 T1 Line Requirements

The following are requirements on the physical line:

a) Each T1 port **shall**[219] be able to operate over any cable length between 0 and 6,000 ft.

b) Each T1 port **shall**[220] incorporate transient protection.

c) Each T1 port **shall**[221] have a jitter tolerance that conforms to [ITU-T Recommendation G.824 (03/93), Section 3.1.1, Table 2].

3.2.2.7.1.3 T1 Time Slots

A single T1 frame contains twenty-four time slots. These slots **shall**[222] be allocated according to the following subparagraph. Table 3-16, Fractional T1 Format, summarizes the time slot and channel allocation being used across the MDR/RIU interface.

Table 3-16. Fractional T1 Format

Time Slot Number	Data Allocation	
1	*Timing Channel*	16-bit Counter LSB
2		16-bit Counter MSB
3	*Spare*	TBD
4		
5	*Data Channel 1*	HDLC # 1
6		
7		
8		
9	*Data Channel 2 [if used]*	HDLC # 2
10		
11		
12		
13	*Data Channel 3 [if used]*	HDLC # 3
14		
15		
16		
17	*Data Channel 4 [if used]*	HDLC # 4
18		
19		
20		
21	*Data Channel 5 [if used]*	HDLC # 5
22		
23		
24		

3.2.2.7.1.3.1 T1 Time Slot Assignments

The T1 time slots are allocated in the following manner:

a) Time slots one and two **shall**[223] be used to carry information in a timing channel.

b) Time slots three and four **shall**[224] be unused, and designated as spares.

c) The remaining time slots (5 through 24) in the T1 frame **shall**[225] be organized into five data channels, each consisting of four contiguous T1 time slots.

d) The MDR will be configurable to use any one of the five data channels plus the timing channel (slots 1 and 2). The default data channel **shall**[226] be channel 1 (slots 5 - 8).

3.2.2.7.1.3.2 Timing Channel

The following describes the characteristics of the Timing Channel:

a) Timing **shall**[227] be conveyed in the timing channel using a 16-bit counter that increments by one for each T1 frame.

b) The first timing slot **shall**[228] contain the low-order least significant byte (LSB) of the counter with the most significant bit of the byte transmitted/received first.

c) The second timing slot **shall**[229] contain the high-order most significant byte (MSB) of the counter with the most significant bit of the byte transmitted/received first.

d) Bit 1 (least significant bit) of each HDLC message octet **shall**[230] be the first bit transmitted over the Data Channel on the T1 line. Note that due to HDLC zero-bit insertion, HDLC message octets will not necessarily be aligned on T1 time slot boundaries. In addition, HDLC Frames will not necessarily begin transmission or reception in the first bit of a T1 time slot.

e) The RIU Timing Channel counter will be set to a value of zero at each VDL Mode 3 6-second epoch.

f) The MDR will loop-back to the RIU the information contained in the Timing Channel every T1 frame. The looped back Timing Channel will be delayed in the MDR by a constant time up to 1 millisecond. The MDR Timing Channel loop-back will be required by the RIU when measuring the round trip time delay through an unknown path (e.g., Telco T1) between the RIU and the MDR.

g) The MDR will derive all necessary VDL Mode 3 TDMA timing information using the Timing Channel, T1 frame timing, and the MAC Timing Offset Correction messages provided by the RIU. The MDR is responsible for incorporating the necessary corrections to compensate for internal delays within the radio (e.g., processing delays, FIR filter delays, modulation delays, demodulation delays).

h) In remote connections using asynchronous clocks, there exists the possibility that the elastic stores will repeat, or skip a frame, to accommodate clock slippage. Each MDR will be responsible for detecting this error condition and reporting it to the RIU.

i) The RIU will estimate the propagation delay for each T1 port using the data in the timing slots looped-back by the MDRs.

3.2.2.7.1.3.3 T1 Data Channels

The following describes the characteristics of the Data Channels:

a) Each data channel will be dedicated to one HDLC link.

b) Each data channel **shall**[237] be capable of carrying data, control, monitoring and status information in the VDL Mode 3 and PCM Voice, control, monitoring and status information in the DSB-AM Mode.

c) Allocation of time slots to channels **shall**[238] be fixed for all T1 frames on a given link (i.e., for as long as a channel is in use, it occupies the same time slot numbers in each T1 frame that is generated).

3.2.2.7.1.4 T1 Performance Monitoring

3.2.2.7.1.4.1 Severely Errored Second

The line will be considered in a 'severely errored second' if there are more than 100 ESF CRC-6 failures in a second.

3.2.2.7.1.4.2 Burst Failure

Six (6) consecutive severely errored seconds will indicate a line failure.

3.2.2.7.1.4.3 Short Term Failure

A failure will also be indicated if there are more than ten (10) severely errored seconds in a five-minute interval.

3.2.2.7.1.4.4 Long Term Failure

The system will declare a failure if 99.9675% of the seconds (> 28) are not error-free, computed as a moving average over a 24 hour time period. This equates to a daily average BER of 10^{-6}.

3.2.2.7.2 System Timing

a) Maintaining accurate timing across the MDR to RIU interface is critical to the successful operation of VDL Mode 3. Timing information is required by the transmitter to properly generate the bursts within the predefined transmission window. Timing information is needed by the receiver to perform a synchronization search centered on the nominal burst position. The leading edge of the framing bit **shall**[244] be the point-of-reference for system timing.

b) The RIU will be the source of system timing.

c) The leading edge of a framing bit of T1 frame **shall**[245] coincide with the beginning of the VDL Mode 3 6-second epoch within plus or minus 10 microseconds.

d) The RIU will implement any corrections to the T1 clock and framing rate in such a way that no clock pulses are added or skipped and jitter requirements are met, so that synchronism is maintained at the T1 ports.

e) Figure 3-85 shows the timing relationship between the VDL Mode 3 6-second epoch boundary, the T1 frame timing, the Time of Arrival (TOA)/Time of Transmission

(TOT) message timing reference and the first MAC cycle within an epoch. The start of the 6-second epoch **shall**[246] coincide with the center of the first D8SPK synchronization symbol in LBAC 1 of slot A in the even TDMA frame of the first MAC cycle in the epoch, which is also –1260 D8PSK symbol periods relative to the MAC cycle "0" Timing Reference Point (TRP) as defined in the VDL Mode 3 RTCA DO-224a.

f) For Voice-Burst, Data-Burst and Management-Burst Messages, the TOT and TOA fields **shall**[247] have a "0" reference point that corresponds to the center of the first D8PSK synchronization symbol in LBAC 1 of slot A in the even TDMA frame of the first MAC cycle in the VDL Mode 3 epoch in which the burst is transmitted or received. Note that the ramp-up interval of the burst begins 5.5 D8PSK symbol periods prior to the time indicated by the TOA/TOT field.

g) For the Sync Search Control Message, the Sync Search Start (S_START) field **shall**[269] define the earliest time within a VDL Mode 3 epoch where the center of the first D8PSK synchronization symbol in a receive burst may occur.

h) For the Sync Search Control Message, the Sync Search Stop (S_STOP) field **shall**[270] define the latest time within a VDL Mode 3 epoch where the center of the first D8PSK synchronization symbol in a receive burst may occur.

i) The resolution of the TOA, TOT, S_START and S_STOP fields **shall**[293] be 1/16th of a D8PSK symbol period and **shall**[271] have a range of 0 to 1,007,999 within a 6-second VDL Mode 3 epoch.

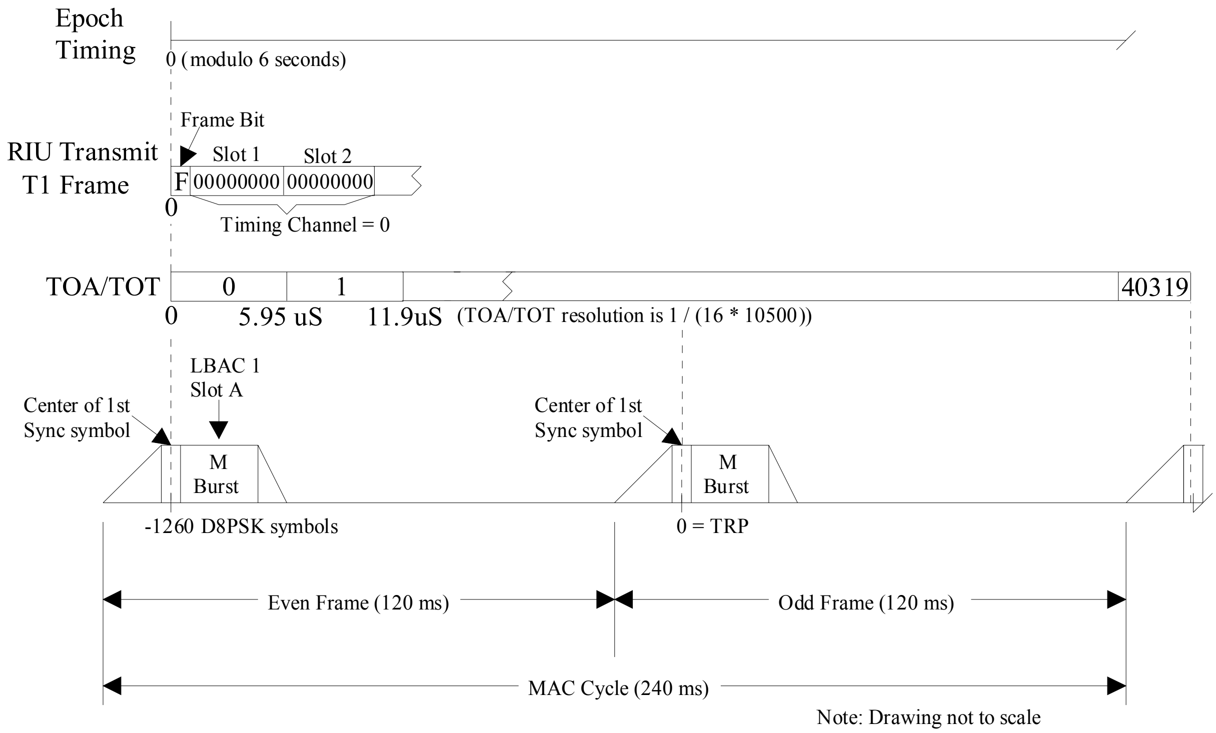


Figure 3-85. VDL Epoch, T1 and MAC Cycle Timing

3.2.3 Analog-type Interface (NA)

3.2.4 Discrete-type Interface (NA)

3.2.5 Interface Design Characteristics Table

Table 3-17, the Interface Design Characteristics table, provides a reference to all messages that traverse across the RIU-MDR Transmitter and RIU-MDR Receiver interface.

Table 3-17. Interface Design Characteristics

Message	Paragraph	Size (Octets)	Source	Destination	HDLC Frame Type
Test Command	3.2.2.6.2.1	4	RIU RIU	MDR TX MDR Receiver	Test
Test Response	3.2.2.6.2.1	4	MDR TX MDR RX	RIU RIU	Test
Link Clearing (Test Command / Response)	3.2.2.6.2.3	5/4	RIU RIU MDR TX MDR RX	MDR TX MDR RX RIU RIU	Test
Voice-Burst	3.2.2.6.5.1.1	Variable	RIU MDR RX	MDR TX RIU	UI
Data-Burst	3.2.2.6.5.1.2	Variable	RIU MDR RX	MDR TX RIU	UI
Management-Burst (All Management-Burst with the exception of 3T Handoff-Check Burst)	3.2.2.6.5.1.3	Variable	RIU MDR RX	MDR TX RIU	UI
3T Handoff-Check Burst (Management-Burst)	3.2.2.6.5.1.3	12	RIU MDR RX	MDR TX RIU	UI
Sync Search Control	3.2.2.6.5.1.4	6	RIU	MDR RX	UI
PCM Voice	3.2.2.6.5.1.5	Variable	RIU MDR RX	MDR TX RIU	UI
Radio Control	3.2.2.6.5.1.6	Variable	RIU RIU MDR TX MDR RX	MDR TX MDR RX RIU RIU	UI
Radio Monitoring	3.2.2.6.5.1.7	Variable	RIU RIU MDR TX MDR RX	MDR TX MDR RX RIU RIU	UI
RIU/MDR Status	3.2.2.6.5.1.8	2	MDR TX MDR RX	RIU RIU	UI

3.3 Physical Design Characteristics

The following subsections are used to define the physical characteristics of the MDR/RIU Interface.

3.3.1 Electrical Power/Electronic Characteristics

3.3.1.1 Connectors

The T1 cables to the MDR transmitter and MDR receiver will connect via RJ-48 connectors as per the Code of Federal Regulations, Title 47, Section 68.502(e).

3.3.1.2 Wire/Cable

The T1 specifications require the use of ABAM-100 ohm balanced cabling.

3.3.1.3 Electrical Power/Electronic Referencing (Grounding)

NA

3.3.1.4 Fasteners

NA

3.3.1.5 Electromagnetic Compatibility

NA

4. QUALITY ASSURANCE PROVISIONS

4.1 General

The interface requirements imposed by section 3 of this ICD shall be verified by use of the verification methods specified in paragraph 4.4. Verification methods and levels shall be applied in accordance with Appendix F, Table F-1, Verification Requirements Testability Matrix (VRTM).

4.2 Responsibility for Verification

FAA management has the responsibility for developing and implementing the verification of requirements for each project. FAA management may also delegate verification activities to other FAA organizations, independent contractors, and/or the prime project contractor.

4.3 Reserved

4.4 Verification Methods

The four verification methods that can be utilized in measuring equipment performance and compliance of requirements are as follows.

a) **Inspection** – Inspection is a method of verification to determine compliance without the use of special laboratory equipment, procedures, or services and consists of non-destructive static-state examination of hardware, software, and/or technical data and documentation.
b) **Test** – Test is a method of verification wherein performance is measured during or after the controlled application of functional and/or environmental stimuli. Quantitative measurements are analyzed to determine the degree of compliance. The process uses standardized laboratory equipment, procedures and/or services.
c) **Demonstration** – Demonstration is a method of verification where qualitative determination of properties is made for a configuration item, including software and/or the use of technical data and documentation. The items being verified are observed, but not quantitatively measured, in a dynamic state.
d) **Analysis** – Analysis is a method of verification where hardware or software designs are compared with known scientific and technical principles, procedures, and practices to estimate the capability of the proposed design to meet the mission and system requirements.

5. PREPARATION FOR DELIVERY

NEXCOM equipment will be delivered in accordance with section F of the contract/SOW.

6.0 NOTES

6.1 Notes on Information Items

The contents of this Section are for informational purposes only and are not a part of the requirements of this specification. They are not contract requirements nor binding on either the Government or the Contractor. In order for these terms to become a part of the resulting contract, they must be specifically incorporated in the schedule of the contract. Any reliance placed by the Contractor on the information in these Subsections is wholly at the Contractor's own risk.

6.2 Applicable Definitions

6.2.1 Very High Frequency (VHF)

In this document the term VHF applies specifically to the frequency range 112.000 MHz – 137.000 MHz, the frequency range reserved for Aeronautical Mobile (Route) Service.

6.2.2 Ultra High Frequency (UHF)

In this document the term UHF applies specifically to the frequency range 225.000 MHz - 399.975 MHz frequency range, the frequency range reserved for military, navigation and communications.

6.2.3 Mean Time Between Failures (MTBF)

A basic measure of reliability for non-repairable items: the total number of life units of an item divided by the total number of failures within that population, during a particular measurement interval under stated conditions.

6.2.4 Mean Time To Repair (MTTR)

A basic measure of maintainability: the sum of corrective maintenance times at any specific level of repair, divided by the total number of failures within an item repaired at that level, during a particular interval under stated conditions.

6.2.5 Duty Cycle

The percentage of time that the transmitter is keyed in proportion to total service time.

6.2.6 Line Replaceable Unit (LRU)

An item which may consist of a unit, an assembly (circuit card assembly, electronic component assembly, etc.), a subassembly, or a part, that is removed and replaced at the site maintenance level in order to restore the system/equipment to operational status.

6.2.7 Co-channel Interference

The power ratio of the wanted signal level to the unwanted signal level at the specified voice quality is the co-channel interference protection in dB (positive value). The co-channel interference protection for Mode 3 data /digitized voice is the overall capability of a receiver to demodulate a signal properly (to achieve a defined BER performance) in the presence of an unwanted modulated signal at the same assigned frequency. The co-channel interference protection for DSB-AM voice is the overall capability of the receiver to provide intelligible voice in the presence of an unwanted modulated signal at the same assigned frequency. The co-channel interference requirement has a major impact on frequency re-use planning criteria.

6.2.8 Adjacent Channel Emissions

Adjacent channel emissions are interference signals resulting from modulated RF signal power transmitted that are outside of the assigned channel. Adjacent channel emissions include discrete frequency spurious signals, and noise like signals (including phase noise) at the transmitter output.

6.2.9 Bit Error Rate

The BER corresponds to the uncorrected bit error probability and is expressed as the ratio of the number of incorrect bits received to the number of bits received without benefits of Forward Error Correction (FEC).

6.2.10 Initialization

Initialization (also cold start) occurs when (a) the receiver or transmitter is first turned on when delivered from the factory, an (b) when the initialization function is activated. A result of the initialization function is that all control parameters return to their default values.

6.2.11 ABAM

ABAM refers to a certain construction of cable, which is plastic-insulated cable (PIC) waterproof, pulp air core or PIC riser, with polyethylene or poly vinyl chloride (PVC) conductor insulation, 22 American Wire Gauge (AWG) with an aluminum/vinyl jacket. Other letter designators indicate other components and characteristics. ABAM is most often used for T1 data connections by long-haul data companies, regional bell operating companies (RBOCs) and common carriers.

6.2.12 MDR RF Output

The transmitter connector to which the antenna would be connected in a particular configuration.

6.2.13 MDR RF Input

The receiver connector to which the antenna would be connected in a particular configuration.

APPENDIX A. List of Acronyms

The following acronyms and abbreviations apply to the terms used in this ICD:

Acronym	**Definition**
μs	microseconds
AD	Address
AGC	Automatic Gain Control
AM	Amplitude Modulation
ANSI	American National Standards Institute
ATC	Air Traffic Control
B8ZS	Bipolar 8-Zero Substitution
BER	Bit Error Rate
CMIP	Common Management Information Protocol
CN	Control
codec	Coder/Decoder
CRC	Cyclic Redundancy Check
CTYPE	Control/Monitoring Type
DACS	Digital Access Cross-Connect Switch
D8PSK	Differential 8 Phase Shift Key
dB	Decibel
dBm	Power level in decibels relative to 1milliWatt
DF	R-S Coded Data
DH	Data Header
DSB	Double Sideband
EOM	End of Message
ER	Error indication on Reply
ESF	Extended Super Frame
F	Flag
FAA	Federal Aviation Administration
FCC	Federal Communications Commission
FCS	Frame Check Sequence
FEC	Forward Error Correction
GEC	Golay Error Count
GNI	Ground Network Interface
GSC	Ground Station Code
HDLC	High-Level Data Link Control
ICAO	International Civil Aviation Organization
ICD	Interface Control Document
I	Information
ID	Identification
ISO	International Organization for Standardization
ITU-T	International Telecommunications Union Telecommunication Standardization Sector
JRC	Joint Resource Council
kHz	kilo Hertz

Acronym	Definition
LBAC	Logical Burst Access Channel
LDRCR	Low Density Radio Communications Link
LEN	Length (of Segment)
LRU	Line Replaceable Unit
lsb	least significant bit
LSB	Least Significant Byte
MAC	Media Access Control
MASPS	Minimum Aviation System Performance Standards
MDR	Multimode Digital Radio
MDT	Maintenance Data Terminal
MHz	Mega Hertz
M/S	Main/Standby
ms	milliseconds
msb	most significant bit
MSB	Most Significant Byte
MSG	Message
MUX	Multiplexer
nmi	Nautical Mile
NEXCOM	Next-Generation Air/Ground Communications
OSI	Open Systems Interconnection
PCM	Pulse Coded Modulation
PID	Protocol Identifier
PLL	Phase-Locked Loop
PTT	Push To Talk
PV	PCM Voice
PWR	Power
RCE	Radio Control Equipment
RCF	Radio Control Facility
RF	Radio Frequency
RIU	Radio Interface Unit
RMM	Remote Maintenance and Monitoring
RR	Request/Reply
R-S	Reed-Solomon
RMMC	Remote Maintenance Monitoring and Control
RTN	Return To Normal
RX or Rx	Receiver
SARPS	Standards and Recommended Practices
SC	Segment Count
SID	Slot Identifier
SINAD	Signal-to-Noise and Distortion
SN	Sequence Number
SRD	System Requirements Document
SOW	Statement Of Work
STYPE	Synchronization Header Type
TBD	To Be Determined

Acronym	**Definition**
TDM	Time Division Multiplexed
TDMA	Time Division Multiple Access
TOA	Time of Arrival
TOT	Time of Transmission
T/R or TX/RX	Transmitter/Receiver
TRP	Timing Reference Point
TSC	Total Segment Count
TX or Tx	Transmitter
UI	Un-numbered Information
V/D	Voice/Data
VDL	VHF Digital Link
VF	Voice Frame
VFSN	Voice Frame Serial Number
VH	Voice Header
VHF	Very High Frequency
VRTM	Verification Requirements Testability Matrix
VSWR	Voltage Standing Wave Ratio
W	Watt

APPENDIX B. T1, GPS and MAC Timing for the VDL Mode 3 Ground Radio System

Figure B-1 shows the timing relationship between GPS time, the T1 frame timing and 1.544 MHz clock, the T1 Timing Channel (first two time slots), the Time of Arrival (TOA) /Time of Transmission (TOT) reference counter in the MDR, and the MAC burst timing.

In the example shown in Figure B-1, the 6-second VDL Mode 3 epoch N begins coincident with the active edge of the GPS 1 Pulse Per Second (PPS) signal as the GPS seconds counter counts from 5 to 6. Whenever the GPS time of day seconds value becomes 0 modulo 6 at the RIU, the active edge of the associated GPS 1 PPS signal is aligned with the leading edge of the transmit T1 framing pulse in the RIU plus or minus 10 microseconds (μs).

The TOA/TOT reference counter is clocked at 168 kHz (16 x 10,500) and counts modulo 1,008,000 (one 6-second VDL Mode 3 epoch). The MDR relies on the TOA/TOT reference counter to provide an accurate timing reference for VDL Mode 3 burst modulation/demodulation. The first two time slots in the T1 transmit frame on the RIU-to-MDR link, along with the T1 framing reference and the Timing Offset Correction value provided by the RIU are all used to convey the MAC timing reference to the MDR. The first two T1 time slots are called the "Timing Channel" and consist of a 16-bit binary counter that is reset to 0 at the start of each VDL Mode 3 6-second epoch, and counts up by one on the leading edge of each T1 frame pulse. T1 time slot 1 carries the 8 least significant bits of the 16-bit Timing Channel word, with the most significant bit of the byte transmitted first. Likewise, T1 time slot 2 carries the 8 most significant bits of the 16-bit Timing Channel word, with the least significant bit of the byte transmitted last. In the MDR, the TOA/TOT reference counter is reset to zero on the leading edge of the receive T1 framing pulse that precedes the Timing Channel value of 0000. In the example shown in Figure B-1, the Timing Channel word is shown at the end of VDL Mode 3 epoch N-1 (Timing Channel word = 47,999) and one T1 frame later at the start of VDL Mode 3 epoch N (Timing Channel word = 0).

Figure B-1 also shows the timing of a downlink M-burst for an aircraft co-located with the ground receiver (range = 0, Timing Offset Correction = 0). In this case, the center of the 1st D8PSK sync symbol is aligned with the start of 6-second epoch N. For a non-co-located aircraft, the value of the TOA/TOT reference counter that coincides with the center of the 1st D8PSK sync symbol received (referenced to the antenna port) is non-zero and represents the "Time of Reception" within a 6-second VDL Mode 3 epoch in the MDR receiver.

The Primary Timing Responsibilities of the RIU include the following:

a) Generate the leading edge of the T1 framing pulse such that, on one second time boundaries, it coincides with the active edge of the GPS 1 PPS signal (within ± 10 μs),

b) Generate transmit Timing Channel data in the first two T1 time slots, with the Timing Channel 16-bit word reset to 0 at the start of each VDL Mode 3 6-second epoch,

c) Measure the round trip delay on the looped-back T1 Timing Channel from an MDR and issue Timing Channel Correction messages to MDR(s), and

d) Monitor the receive T1 framing pulse and Timing Channel from the MDR for T1 timing anomalies (e.g., T1 frame insertion / deletion or interval between T1 frame pulses not 125 μs).

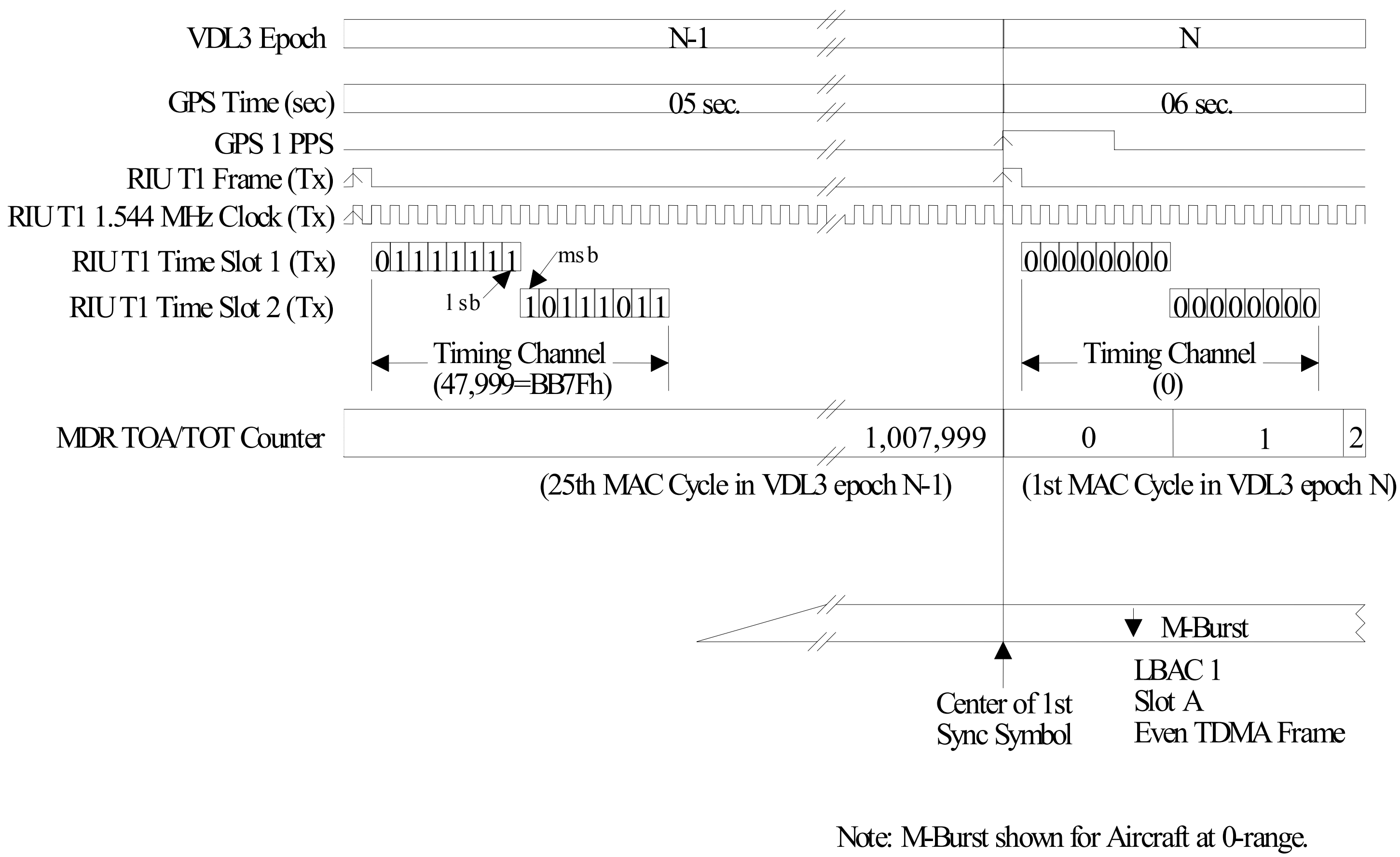


Figure B-1. GPS, T1 and MAC Timing Relationships

The RIU may calculate the round trip delay to a specific MDR by measuring the time interval between an RIU T1 transmit frame pulse associated with RIU transmit Timing Channel N, and the RIU T1 receive frame pulse associated with RIU receive Timing Channel N , and subtracting the MDR specified loop back delay, T_{TCL} which is a constant delay between 0 and 1 millisecond. In this example, the distance between the RIU and the MDR is four nautical miles, resulting in a one-way propagation delay of approximately 25 μs over the T1 line. In Figure B-2a, the MDR has its Timing Offset Correction set to 0, which results in a +25 μs error in the MDR TOA/TOT reference counter. This example presumes that the RIU makes a round trip Timing Channel measurement and sends a Timing Offset Correction message back to the MDR with a correction value of 25 μs. Figure B-2b shows the corrected TOA/TOT reference counter timing at the start of the next VDL Mode 3 6-second epoch. It should be clear from this example that the T1 propagation path between the RIU and the MDR should be symmetrical, i.e. the propagation delay on the RIU-to-MDR T1 link should be the same as the propagation delay on the MDR-to-RIU T1 link.

If an RIU is controlling multiple MDRs, only one MDR can report back on the Timing Channel, and the RIU can only measure the precise delay to that MDR. In cases where the multiple MDRs are not co-located, the distance between the T1 multiplexer equipment and each MDR should be established at installation time. The RIU will then adjust the Timing Offset Correction values individually for each MDR at run time.

The Primary Timing Responsibilities of the MDR include the following:

a) Generate a local TOA/TOT reference counter from information provided by the receive T1 clock and framing signals, the receive Timing Channel word and the Timing Offset Correction value provided by the RIU.

b) Loop back the received T1 clock and framing pulse on the Transmit T1 link back to the RIU.

c) Loop back the received Timing Channel word from the RIU and transmit to the RIU with a constant delay of T_{TCL} +/- 10 microseconds, where $T_{TCL} <= 1$ millisecond.

d) Monitor the receive T1 framing pulse and Timing Channel & detect T1 timing anomalies. When timing anomalies are detected on the T1 line from the RIU, disconnect the MDR from the antenna port or insert attenuation until system timing with the RIU is re-established. This should be done to protect the front end of MDR receivers that may be co-located with MDR transmitters.

Note that the looped back T1 transmit timing in the MDR is not subjected to the Timing Offset Correction provided by the RIU. The Timing Offset Correction only applies to the generation of the local TOA/TOT reference counter.

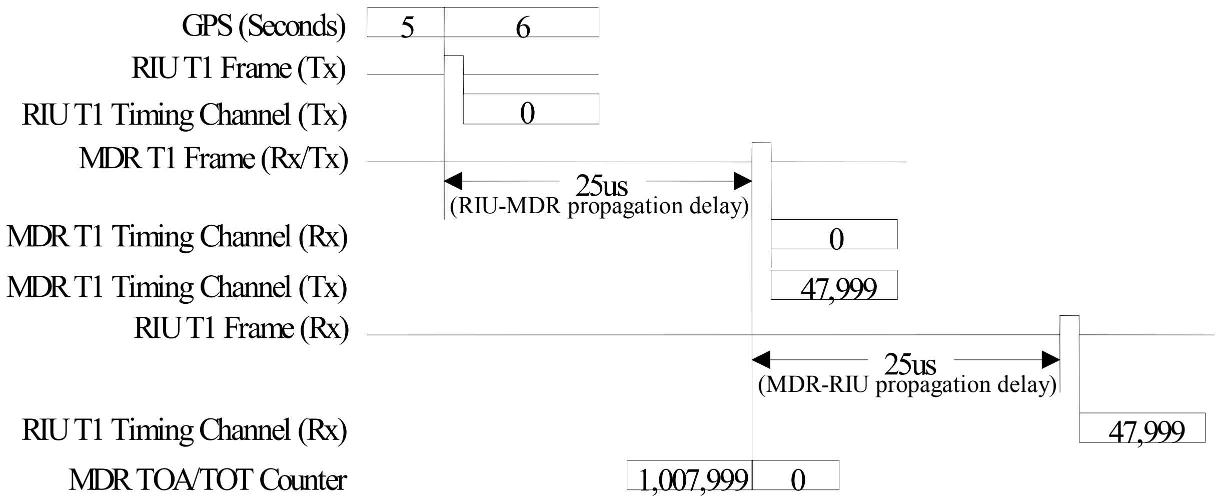


Figure B-2a. T1/MAC Timing with MDR Timing Offset Correction = 0

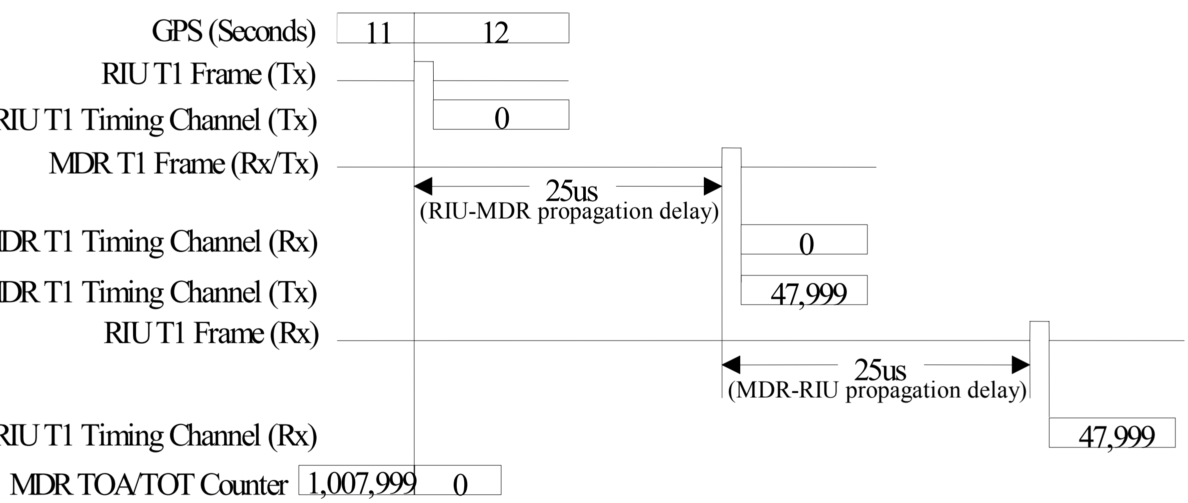


Figure B-2b. T1/MAC Timing with MDR Timing Offset Correction = 25μs

APPENDIX C. NEXCOM VDL DSB-AM PCM Message Timing

C.1 Introduction.

This appendix discusses some of the timing problems associated with sending DSB-AM PCM voice packets between the RIU and the MDR and offers a candidate solution. It is assumed that the packet timing in both the MDR and the RIU is derived from a 5ppm or better clock source. It is also assumed that the PCM coder/decoder (codec) resides in the RIU.

C.2 PCM Background.

PCM data packets will be sent over the HDLC data link using four T1 time slots, with a throughput rate of 256 kbps. It will be necessary to occasionally send other HDLC packets (status, control, monitoring) during PCM voice transmissions. It is likely that the DSP or control microprocessor in the RIU/MDR will incur some variable delay (due to multitasking, interrupt latency, other HDLC message transmission, etc.) as it prepares each segment of speech for transmission/reception over the T1 link. Therefore, the timing between successive PCM packet transmissions could vary significantly.

C.3 PCM Timing

In order to insure that voice underflow does not occur, the recipient processor (MDR transmitter for uplink voice, RIU for downlink voice) will be required to initially buffer more than one PCM message at the start of a voice message, before using the voice bits in the first PCM message. To avoid problems associated with processing partial HDLC messages (i.e. processing a partial PCM message before the entire PCM HDLC message has been received), we will buffer an integral multiple (2 or more) of complete PCM messages.

Figure C-1 shows a theoretical worst case timing scenario for an uplink DSB-AM voice transmission. In this example, the first two PCM messages incur no processing delay in either the RIU ($T_{RIU} = 0$) or the MDR ($T_{MDR} = 0$). The MDR begins modulating the PCM voice $2*T_{VF} + T_{T1}$ seconds after the beginning of the first voice frame, which would result in a minimum voice delay in the ground link.

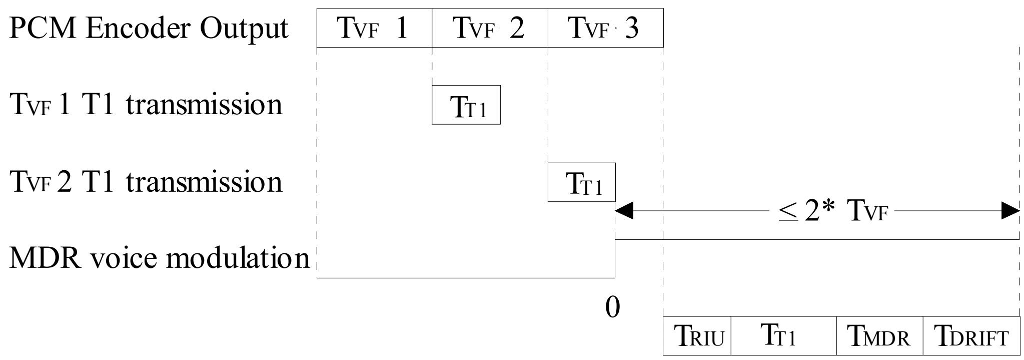
In our worst case example, the third PCM message incurs the maximum delay of:
$T_{RIU} + T_{T1} + T_{MDR}$

When the MDR transmitter begins modulating DSB-AM voice, it has enough data buffered to send voice for $2*T_{VF}$ seconds. But the RIU must wait $T_{VF} – T_{T1}$ seconds for arrival of the third complete PCM voice frame before it can be sent to the MDR transmitter. Allowing T_{DRIFT} seconds to account for cumulative clock drift in the RIU and MDR, the following equations can be used to establish the minimum duration of a PCM voice frame (T_{VF}):

$$T_{VF} – T_{T1} + T_{RIU} + T_{T1} + T_{MDR} + T_{DRIFT} \leq 2*T_{VF} \qquad \text{(equation 1)}$$

which reduces to,

$T_{RIU} + T_{MDR} + T_{DRIFT} \leq T_{VF}$ (equation 2)



T_{VF} = Duration of a PCM voice frame
T_{RIU} = Time it takes RIU to process one PCM encoder frame and to format and send one maximum length non-PCM message over the RIU-MDR T1 link.
T_{T1} = Time to send T_{VF} length PCM voice message over the RIU-MDR T1 link
T_{MDR} = Time it takes MDR to process T_{VF} length PCM message from RIU-MDR T1 link
T_{DRIFT} = Cumulative clock drift allowed before voice under flow occurs

Figure C-1. Worst Case PCM Packet Timing for Uplink Transmission

If we allow for cumulative clock drift (@ 10 ppm) for a maximum contiguous voice transmission of three minutes, then T_{DRIFT} = 1.8 milliseconds (ms). (Note: With a 2 ppm reference in both the RIU and the MDR, the maximum contiguous voice transmission is 7.5 minutes if T_{DRIFT} = 1.8ms). T_{RIU} represents the total CPU processing time to format all HDLC messages and includes the T1 transmission time of a single, maximum length non-PCM message (N1 = 512). In our example, the T_{RIU} starting reference point is the point in time when the third complete PCM voice frame is available from the PCM encoder in the RIU. If we allow for a single maximum length non-PCM message to be sent (512 I-frame bits), the T1 transmission time of that non-PCM message would take approximately 2.2 ms. If we then allow equal CPU processing time of 5.5ms in both the RIU and MDR, we arrive at T_{RIU} = 7.7ms and T_{MDR} = 5.5ms. We can now solve for the minimum T_{VF}:

T_{VF} min. = 7.7ms + 5.5ms + 1.8ms = 15ms.

With the PCM codec in the RIU, the maximum ground voice delay would be:

$2*T_{VF} + T_{RIU} + T_{T1} + T_{MDR} + T_{DRIFT}$ (equation 3) where T_{T1} is the time required to send a 15ms PCM packet (7.9ms). With the above parameters, the maximum ground voice delay (due to both the MDR and the RIU) would be 52.9 ms.

A similar situation exists for downlink voice, where the receive MDR would packetize 15ms intervals of PCM audio and forward them to the RIU. If the PCM decoder hardware resides in the RIU, the RIU would be required to buffer two complete PCM messages before beginning output to the PCM decoder.

If the GNI PCM codec hardware were to be used, then the RIU would forward each PCM packet from the MDR to the GNI with minimum delay. The GNI processor would then be required to buffer two complete PCM messages before beginning to output the downlink voice to the PCM decoder. In this case, T_{VF} would probably need to be increased by an additional amount of time to account for worst case timing variations in the GNI processor and ground communications link. In addition, T_{DRIFT} may also have to be increased, depending on the stability of the PCM clock in the GNI.

In the DSB-AM configuration, the maximum HDLC I-field must be larger for the PCM message than for all other HDLC messages in order to ensure timely delivery of real time PCM data.

C.4 MDR PCM Specifications

The following sections summarize the PCM requirement for the MDR.

C.4.1 DSB-AM PCM Voice Reception

a) The receive MDR will convert demodulated audio to 128 kbps linear Pulse Code Modulation (PCM) (sampled at 8,000 samples per second and encoded with 16 bits per sample) and send PCM messages to the RIU over the T1 link.

b) PCM voice messages sent from the receive MDR to the RIU will have highest priority.

c) With the exception of the last PCM voice packet in a voice reception, all PCM voice packets sent to the RIU will contain the same number of 16-bit PCM samples, N_{PCM}, where: $120 \leq N_{PCM} \leq 200$.

d) The last PCM voice packet in a voice reception sent to the RIU will contain less than or equal to N_{PCM} PCM samples.

e) For N = 1 and N = 2, the receive MDR will complete transmission of the HDLC end FLAG for the Nth PCM message in a downlink DSB-AM voice reception no later than $0.0075 + [(N + 1) * T_{VF}]$ seconds after squelch break, where:

   N = PCM message number since squelch break; N = 1,2,3…
   $T_{VF} = K / 8{,}000$ seconds, and

K = number of PCM samples in the Nth PCM message (LEN field / 16).

f) For N > 2, the receive MDR will complete transmission of the HDLC end FLAG for the Nth PCM message in a downlink DSB-AM voice reception no later than 0.0075 + [(N - 2) * T_{VF}] seconds after the HDLC end Flag for the 2nd PCM message (N = 2) has been transmitted over the T1 link, where:

N = PCM message number since squelch break; N = 3,4,5…
T_{VF} = K / 8,000 seconds, and
K = number of PCM samples in the Nth PCM message (LEN field / 16).

g) For PCM messages, the N1 parameter does not apply and the maximum number of information bits will be limited to 3,264 s.

The minimum PCM frame size is 15 ms (120 PCM samples) in order to provide the MDR and RIU several ms to process each PCM voice frame. The maximum PCM frame size is 25 ms (200 PCM samples), which limits the maximum end-to-end DSB-AM delay to less than 250 ms.

The equation in bullet e) limits the delay from squelch break to the completion of the first two PCM message transmissions to the RIU. With N_{PCM} = 200, the maximum downlink voice delay in the receive MDR is 92.5 ms, which includes 10 ms for squelch break detection. The equation in bullet f: ensures that PCM samples will arrive at the RIU at least 7.5 ms prior to when they are required at the audio output. Paragraph bullet g) limits T1 line blockage due to non-PCM messages to 2.2 ms. Paragraph bullet h) limits the maximum PCM message frame size to 25 ms.

Figures C-2a and C-2b show an example of downlink PCM voice timing, with PCM frame size set to 15 ms. Figure 1a shows the timing when the 1st and 2nd PCM messages are sent late and Figure 1b shows the timing when the 1st and 2nd PCM message are sent as early as possible. In both cases, voice is output in the RIU as soon as the 2nd PCM packet is received, and the 3rd and 4th PCM messages arrive at the RIU at least 7.5ms prior to when the first sample in the message is required at the audio output. If the PCM frame size is increased to the maximum (25 ms), PCM messages will be guaranteed to arrive at the RIU at least 17.5 ms prior to when the first sample in the message is required at the audio output.

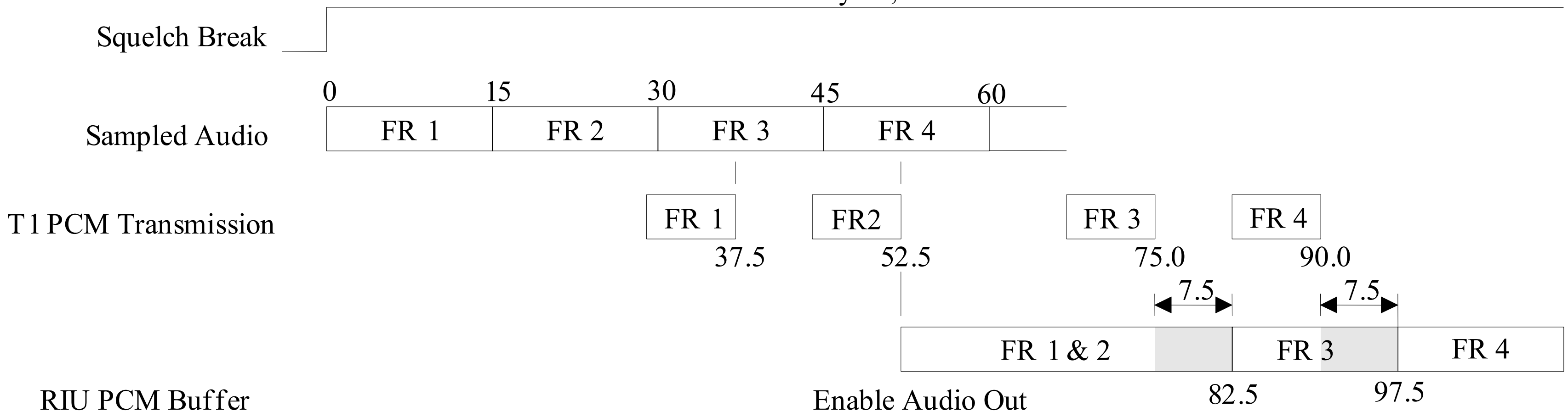


Figure C-2a. Downlink PCM Timing (FR 1&2 late arrival)

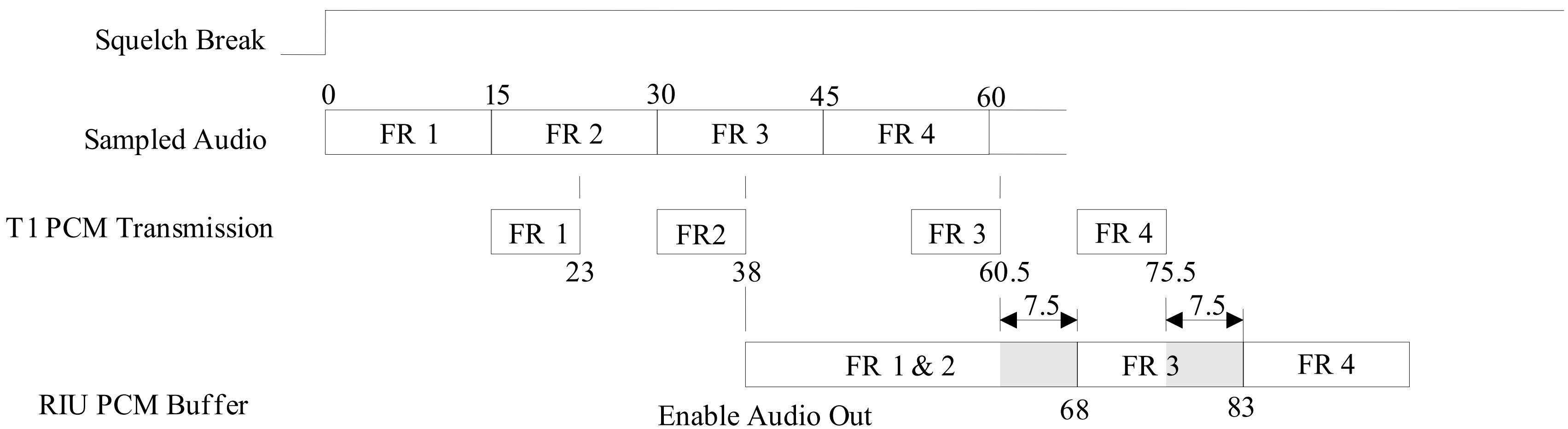


Figure C-2b. Downlink PCM Timing (FR 1&2 early arrival)

C.4.2 DSB-AM PCM Voice Transmission

a) The transmit MDR will convert the PCM stream provided by the RIU to analog audio and perform DSB-AM modulation.

b) At the start of a new uplink PCM voice transmission that requires more than one PCM message (EOM field = 0 in first PCM message), the transmit MDR will begin DSB-AM voice modulation between 0 and 9 ms after the receipt of the second complete PCM message in the voice transmission from the RIU.

c) If the entire voice transmission requires less than two PCM messages (EOM field = 1 in first PCM message), the MDR will begin DSB-AM voice modulation no later than 9 ms after the receipt of the PCM message HDLC end FLAG from the RIU.

d) After an uplink PCM DSB-AM uplink voice transmission has begun, the MDR will continuously modulate DSB-AM voice, while the HDLC end FLAG for each PCM message is received from the RIU at least 7.5 ms prior to the time when the first PCM sample in the PCM message is required to be modulated.

Bullets b) & c) limit the transmit MDR PCM voice delay to a maximum of 9 ms. Bullet d) requires the MDR to continuously modulate DSB-AM PCM voice as long as PCM messages are received from the RIU at least 7.5 ms prior to when the 1st sample in the message is required to be modulated (PCM frame size 15 ms). If the PCM frame size is increased to the maximum (25 ms), PCM messages will be guaranteed to arrive at the transmit MDR at least 17.5 ms prior to when the first sample in the message is required to be modulated.

C.5 RIU PCM Specifications

C.5.1 DSB-AM PCM Voice Reception

a) The RIU will convert the 128 kbps linear PCM stream provided by the receive MDR to analog audio.

b) At the start of a new downlink PCM voice reception that requires more than one PCM message (EOM field = 0 in first PCM message), the RIU will begin outputting DSB-AM analog audio between 0 and 9 ms after the receipt of the second complete PCM message in the voice reception from the MDR.

c) If the entire DSB-AM voice reception requires less than two PCM messages (EOM field = 1 in first PCM message), the RIU will begin outputting analog audio no later than 9 ms after the receipt of the PCM message HDLC end FLAG from the MDR.

d) After a downlink DSB-AM PCM voice reception has begun, the RIU will output continuous audio, while the HDLC end FLAG for each PCM message is received from the MDR at least 7.5 ms prior to the time when voice associated with the first PCM sample in the PCM message appears at the audio output.

Bullets b) & c) limit the RIU receive voice delay to a maximum of 9 ms. Bullet d) requires the RIU to continuously output PCM samples as long as PCM messages are received from the MDR at least 7.5 ms prior to when the 1st sample in the message is required at the audio output (for 15 ms PCM frames). If the PCM frame size is increased to the maximum (25 ms), PCM messages will be guaranteed to arrive at the RIU at least 17.5 ms prior to when the first sample in the message is required at the audio output.

C.5.2 DSB-AM PCM Voice Transmission

a) The RIU will convert analog audio from the RCE to 128 kbps linear PCM format and send PCM messages to the transmit MDR over the T1 link.

b) PCM voice messages sent from the RIU to the transmit MDR will have highest priority.

c) With the exception of the last PCM voice packet in a voice transmission, all PCM voice packets sent to the transmit MDR will contain the same number of 16-bit PCM samples, N_{PCM}, where: $120 \leq N_{PCM} \leq 200$.

d) The last PCM voice packet in a voice transmission sent to the transmit MDR will contain less than or equal to N_{PCM} PCM samples,

e) For N = 1 and N = 2, the RIU will complete transmission of the HDLC end FLAG for the Nth PCM message in an uplink DSB-AM voice reception no later than $0.0042 + [(N + 1) * T_{VF}]$ seconds after the Push-To-Talk signal goes active, where:

   N = PCM message number since PTT, N = 1,2,3…
   T_{VF} = K / 8,000 seconds, and
   K = number of PCM samples in the Nth PCM message (LEN field / 16).

f) For N>2, the RIU will complete transmission of the HDLC end FLAG for the Nth PCM message in an uplink DSB-AM voice reception no later than $0.0075 + [(N - 2) * T_{VF}]$ seconds after the HDLC end Flag for the 2nd PCM message (N = 2) has been transmitted over the T1 link, where:

   N = PCM message number since PTT, N = 3,4,5…
   T_{VF} = K / 8,000 seconds, and
   K = number of PCM samples in the Nth PCM message (LEN field / 16).

g) For PCM messages , the N1 parameter does not apply and the maximum number of information bits will be limited to 3,264 .

The minimum PCM frame size is 15 ms in order to provide the MDR and RIU several milliseconds to process each PCM voice frame. The maximum PCM frame size is 25 ms to limit the maximum end-to-end DSB-AM delay to less than 250 ms.

The equation in bullet e) limits the delay from Push-To-Talk to the completion of the first two PCM message transmissions to the MDR. With N_{PCM} = 200, the maximum uplink PCM voice delay in the RIU is 79.2 ms. The equation in bullet f) ensures that PCM samples will arrive at the MDR at least 7.5 ms prior to when they are required to be modulated. Bullet g) limits T1 line blockage due to non-PCM messages to 2.2 ms. Bullet h) limits the maximum PCM message frame size to 25 ms.

Figures C-3a and C-3b show an example of uplink PCM voice timing, with PCM frame size set to 15 ms. Figure C-3a shows the timing when the 1st and 2nd PCM messages are sent late and Figure C-3b shows the timing when the 1st and 2nd PCM message are sent as early as possible. In both cases, voice modulation begins in the MDR as soon as the 2nd PCM packet is received, and the 3rd and 4th PCM messages arrive at the MDR at least 7.5 ms prior to when the first sample in the message is required by the MDR modulator.

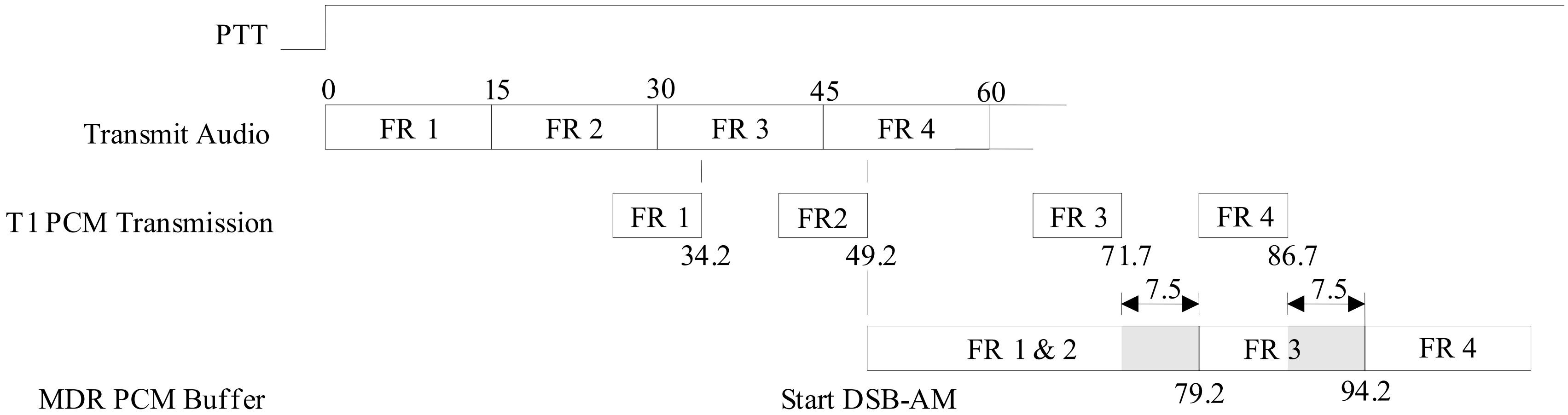


Figure C-3a. Uplink PCM Timing (FR 1&2 late arrival)

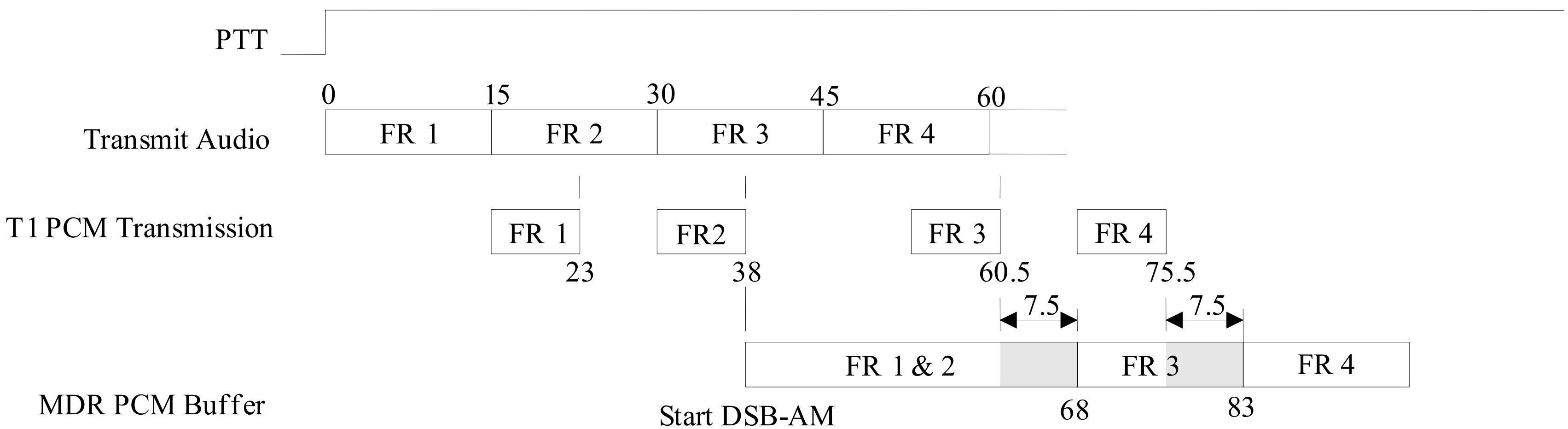


Figure C-3b. Uplink PCM Timing (FR 1&2 early arrival)

APPENDIX D. RIU/MDR HDLC Message Timing

D.1 Downlink Receive Voice Timing

In VDL Mode 3 each Timing State 1 (TS1) and Timing State 3 (TS3) voice burst contains a 24-bit Golay coded header word and six 96-bit vocoder frames of data, where each 96-bit vocoder frame represents 20 milliseconds (ms) of speech. To minimize voice delay, the first vocoder frame received must be sent from the MDR to the RIU as soon as it is demodulated. Some processing time must be allotted both in the MDR and the RIU to format/decode HDLC voice messages and to account for CPU latency. There could also be line blockage on the T1 line (The MDR may have to wait for a maximum length HDLC message to complete transmission before sending the Voice Burst message to the RIU). Variations in message processing delay from time-slot to time-slot must also be accounted for.

Once a VDL Mode 3 voice reception begins, the RIU vocoder data buffer must not underflow. Since the time it takes to process a vocoder frame in both the MDR and the RIU may vary from time-slot to time-slot, there will have to be a requirement in the RIU to delay outputting data to the vocoder at the start of a received voice message. The required RIU delay is:

$$\text{RIU Vocoder Delay} = \frac{\left(\frac{TOA}{16} + 55.5\right)}{10{,}500} + T_{OFF} + T_{RP} + T_{MP} + 0.00394 \text{ seconds,}$$

where:

the RIU Vocoder Delay is the time offset measured from the start of the 6-second VDL Mode 3 epoch in which the burst was received,

TOA is the Time of Arrival within the VDL Mode 3 epoch,

T_{OFF} is the Timing Offset correction value provided to the MDR by the RIU (represents the T1 path delay between the RIU and the MDR),

T_{RP} is the maximum RIU processing time ($T_{RP} < 6$ ms) and

T_{MP} is the maximum MDR receiver processing time ($T_{MP} < 8$ ms).

T_{RP} and T_{MP} will be specified by the RIU and MDR receiver manufacturers with maximum values not to exceed 6 ms and 8 ms, respectively.

In the example shown in Figure D-1, the initial RIU Vocoder Delay is 17.89 ms and includes T_{MP} = 8 ms (maximum) for MDR processing, 2.59 ms for T1 line blockage (N1 parameter = 512, maximum length message with worst case HDLC zero insertion), 0.84

ms to transmit the Voice Burst HDLC message over the T1, T_{RP} = 6 ms (maximum) for RIU processing and 456 microseconds (µs) to cover clock drift and timing drift due to moving aircraft for a message transmission that lasts several minutes.

Note that this RIU delay requirement only applies to the first Voice Burst HDLC message in the VDL Mode 3 voice reception.

D.2 MDR Receiver Voice Timing Requirements:

For the first vocoder frame in a VDL Mode 3 received burst (VFSN = 1), the Voice Burst HDLC message will have the LEN field set to 96, i.e., the first demodulated vocoder frame is not grouped with any other vocoder frames. This requirement is necessary to minimize voice delay.

For VFSN = 1, the MDR receiver will complete transmission of the Voice-Burst message HDLC end FLAG no later than time:

$$T_{RXV1} = \frac{\left(\frac{TOA}{16} + 55.5\right)}{10{,}500} + T_{MP} + 0.00343 \text{ seconds,}$$

where:

T_{RXV1} is the time offset measured from the start of the 6-second VDL Mode 3 epoch in which the burst was received,

TOA is the Time of Arrival as specified in the Voice-Burst message header and.

T_{MP} is the maximum MDR receiver processing time ($T_{MP} < 8$ ms).

The 0.00343 seconds constant in the above equation consists of approximately 2.59 ms for T1 line blockage and 0.84 ms to transmit the Voice Burst HDLC message over the T1 link. Note that the MDR is also required to complete Golay decoding of the Voice Header within the specified time.

The MDR receiver must be capable of continuous demodulation of voice in all time slots. Therefore, even though the data from vocoder frames 2-6 may not be needed until much later, the MDR must complete demodulation of the entire voice burst and finish transmission of all related Voice-Burst messages to the RIU in less than 30 ms for 4-slot configurations (40 ms for 3-slot configurations).

The MDR receiver will send the vocoder frames to the RIU in the order in which they are demodulated.

The MDR receiver will complete transmission of the HDLC end FLAG for the Voice-Burst message that contains vocoder frame 6 no later than time:

$$T_{RXV2\text{-}6} = \frac{\left(\frac{TOA}{16} + 55.5\right)}{10{,}500} + Tslot \text{ seconds,}$$

where:

$T_{RXV2\text{-}6}$ is the time offset measured from the start of the MAC cycle specified by the MAC_CYCL field in the Voice-Burst message header,

TOA is the Time of Arrival as specified in the Voice-Burst message header, and

Tslot = 0.030 for 4-slot configurations and 0.040 for 3-slot configurations.

D.2.1 MDR Receiver M-burst and Data-Burst Timing Requirements

In VDL Mode 3 3-slot configurations, the MDR receiver will complete transmission of the M-Burst message HDLC end FLAG no later than 40 ms (one time slot) after the Time of Arrival (TOA) as specified in the Management-Burst message header.

In VDL Mode 3 4-slot configurations, the MDR receiver will complete transmission of the M-Burst message HDLC end FLAG no later than 30 ms (one time slot) after the Time of Arrival (TOA) as specified in the Management-Burst message header.

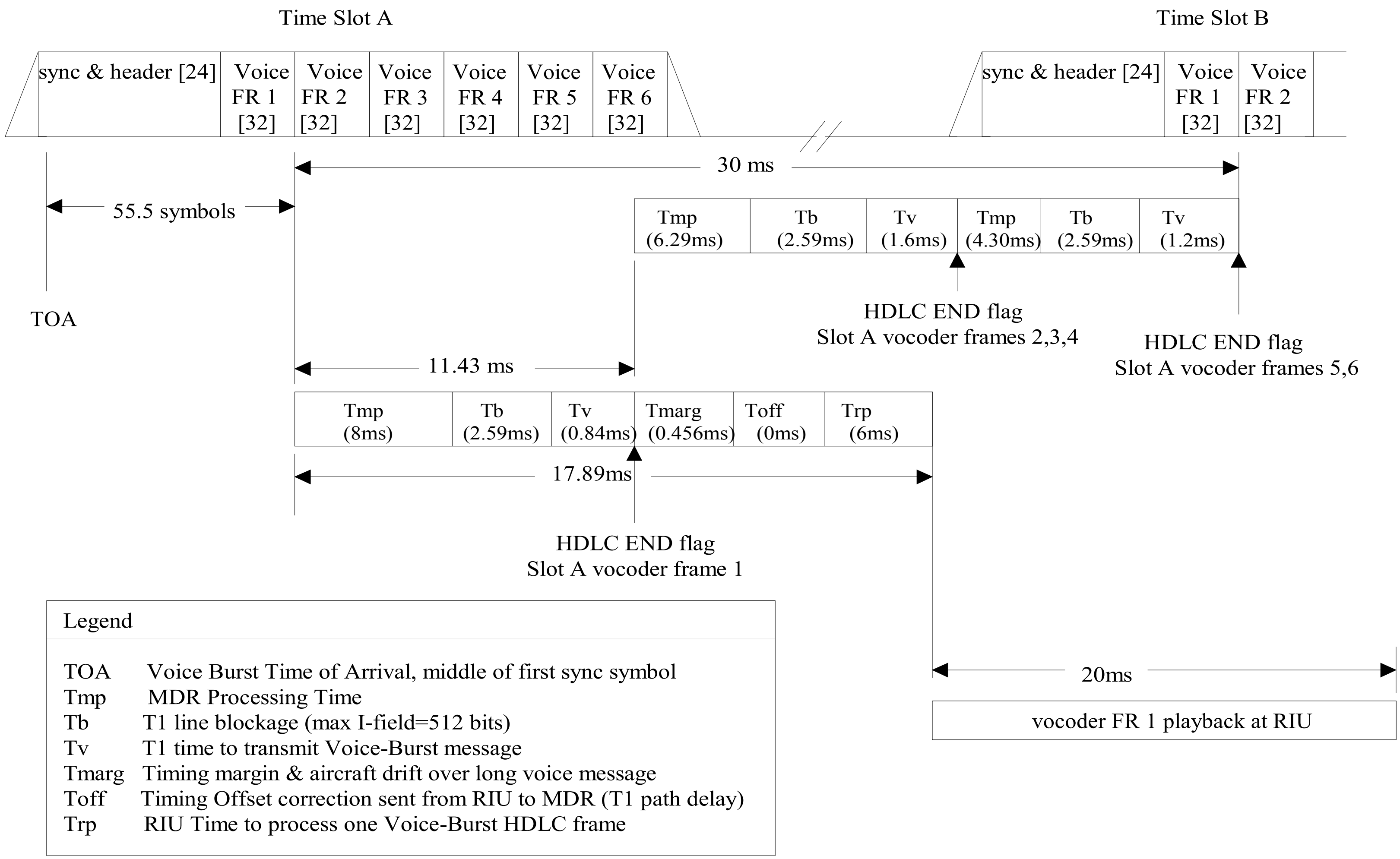
This guarantees prompt delivery of downlink M Acknowledge messages to the RIU and also ensures that the last downlink M-Burst in a MAC cycle will be available to the RIU before the end of the first time slot in the following MAC cycle. The end of the MAC cycle is where the RIU will typically begin building uplink M-Burst messages for the following MAC cycle.

Data-Burst messages will be sent to the RIU in the order in which they are demodulated.

In VDL Mode 3 3-slot configurations, the MDR receiver will complete transmission of the Data-Burst message HDLC end FLAG for the last Data-Burst message segment in a Data burst no later than 40 ms (one time slot) after the Time of Arrival (TOA) as specified in the Data-Burst message header.

In VDL Mode 3 4-slot configurations, the MDR receiver will complete transmission of the Data-Burst message HDLC end FLAG for the last Data-Burst message segment in a Data burst no later than 30 ms (one time slot) after the Time of Arrival (TOA) as specified in the Data-Burst message header.

For Data-Burst messages the MDR must complete demodulation and transmission of all message segments to the RIU within one time slot. However, there is no strict real time requirement on the timing of the first Data-Burst message segment.



notes: 1. numbers in [] brackets are in units of D8PSK symbol periods.
2. ms = milliseconds
3. Drawing not to scale

Figure D-1. MDR-RIU Receive Voice Timing

D.3 Downlink Voice Underflow Problem Example

For the 1st MAC voice burst in a downlink transmission, both the MDR RX and RIU take 0 ms to process (0 ms not probable, but could be close to 0 if MDRs/RIUs are very efficient). In addition, no line blockage occurs on the T1.

For the 2nd downlink voice burst (120 ms later), both the MDR RX and RIU Processors take the maximum (14 ms total), T1 transmission takes 844 µs, and T1 line blockage occurs (2.59 ms) for a total delay of 17.43 ms. (max delays could be due to Interrupt, OS latency, etc).

Problem:

If the RIU begins outputting the 1st vocoder frame in the first burst as soon as it is received, we will end up underflowing voice when the 2nd MAC voice burst message arrives more than 17 ms late.

Possible Solution:

The RIU delays sending output to the vocoder/GNI for T_{MP} ms (maximum MDR receiver processing time as specified by manufacture) + TRP (maximum RIU processing time as specified by manufacture) + 3.43 ms plus an additional 55.5 symbol periods after the TOA indicated by the 1st voice burst in a downlink transmission (plus the Timing Offset correction which is equivalent to the T1 path delay). Subsequent voice packets incur no forced delay in the RIU, the data is simply buffered. This doesn't add to the current timing budgets (except for a few hundred microseconds to account for aircraft movement), it just forces the maximum delay condition all the time. An RIU SSS requirement is needed for this.

Note 1: There are 55.5 symbols from the middle of sync symbol 1 (TOA) to the end of vocoder frame 1.

Note 2: A few hundred extra microseconds are added to account for timing drift of a fast aircraft over a maximum length transmission and to account for T1 link timing variations.

D.4 VDL Mode 3 Uplink Voice, Data and Management Burst Message Timing

Figure D-2 shows the theoretical minimum uplink VDL Mode 3 voice delay. For the ATC-10B vocoder algorithm, the encoder delay is equal to three 20 millisecond vocoder frames, or 60 ms. In the worst case situation, only one 20 ms frame of voice is available at the time the uplink voice burst is transmitted. Thus, the single vocoder frame is transmitted in vocoder frame 6 near the end of the burst and a "silence pattern" is transmitted in the first five vocoder frames. To minimize delay, the vocoder encoder delivers the first vocoder frame at the instant in time when vocoder frame 6 begins modulation in the ground radio. The first vocoder frame transmission is completed (60 ms – 12.2 ms) = 47.8 ms after PTT goes active. Assuming an aircraft at 0-range instantaneously demodulates the first vocoder frame and outputs it to the vocoder, the airborne ATC-10B vocoder incurs a decoder delay of 20 ms. An additional pipeline delay of 100 ms results from the "silence" pattern delivered in the first five vocoder frames. Thus the theoretical minimum uplink voice delay in VDL Mode 3 is:

60.0 ms	ATC-10B encoder delay
-12.2 ms	Time between end of FR1 modulation and start of FR6
+20.0 ms	ATC-10B decoder delay
+100.0 ms	Vocoder frames 1 - 5 (silence pattern)
167.8 ms	**Theoretical minimum VDL Mode 3 Uplink voice delay**

The above calculations assume the 20 ms vocoder frame timing is aligned with the start of modulation for vocoder frame 6, the PTT signal goes active on a 20 ms vocoder frame boundary, and the audio and PTT are available at the radio transmitter with 0 delay through the RIU and T1 line.

This theoretical voice delay is unachievable, since additional time is required for the RIU, MDR and airborne radio to format, modulate/demodulate the vocoder data, and for the Voice-Burst message transmissions over the T1 link. The current uplink voice delay budget limits the voice processing delay in the MDR to 6 ms as illustrated in Figure D-3.

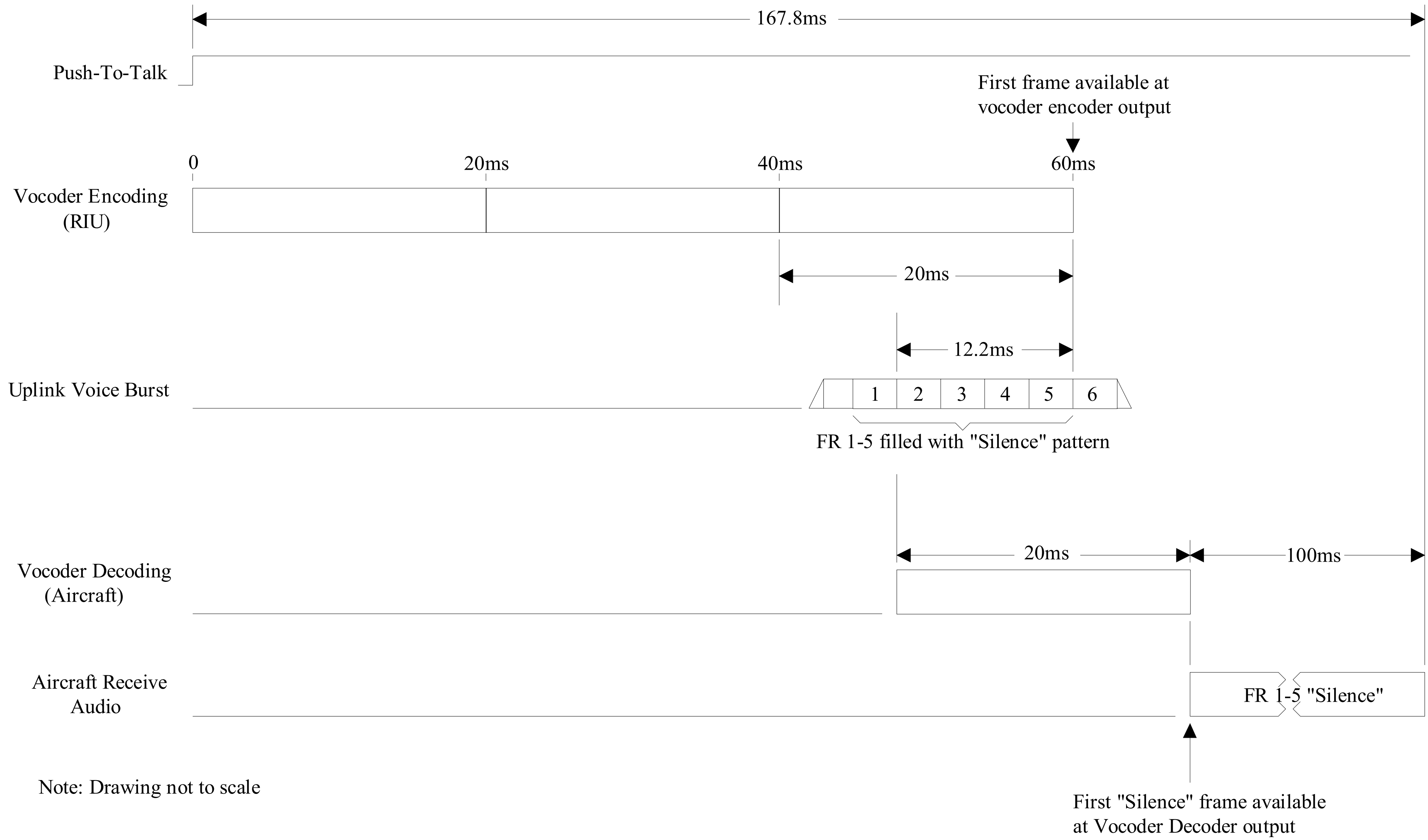
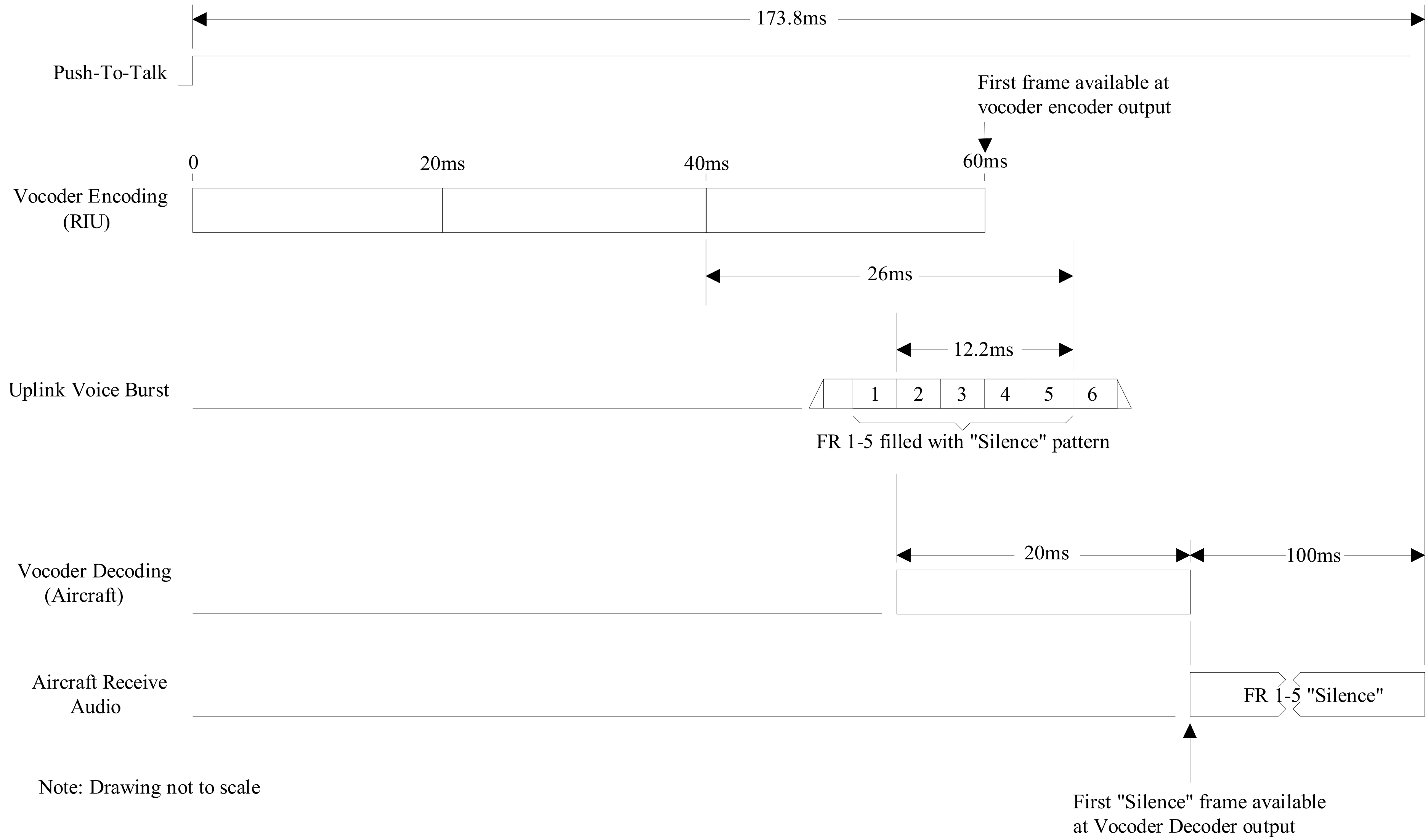


Figure D-2. Theoretical Minimum Uplink Voice Delay in VDL Mode 3



Note: Drawing not to scale

Figure D-3. Uplink Voice Delay, MDR delay = 6 milliseconds

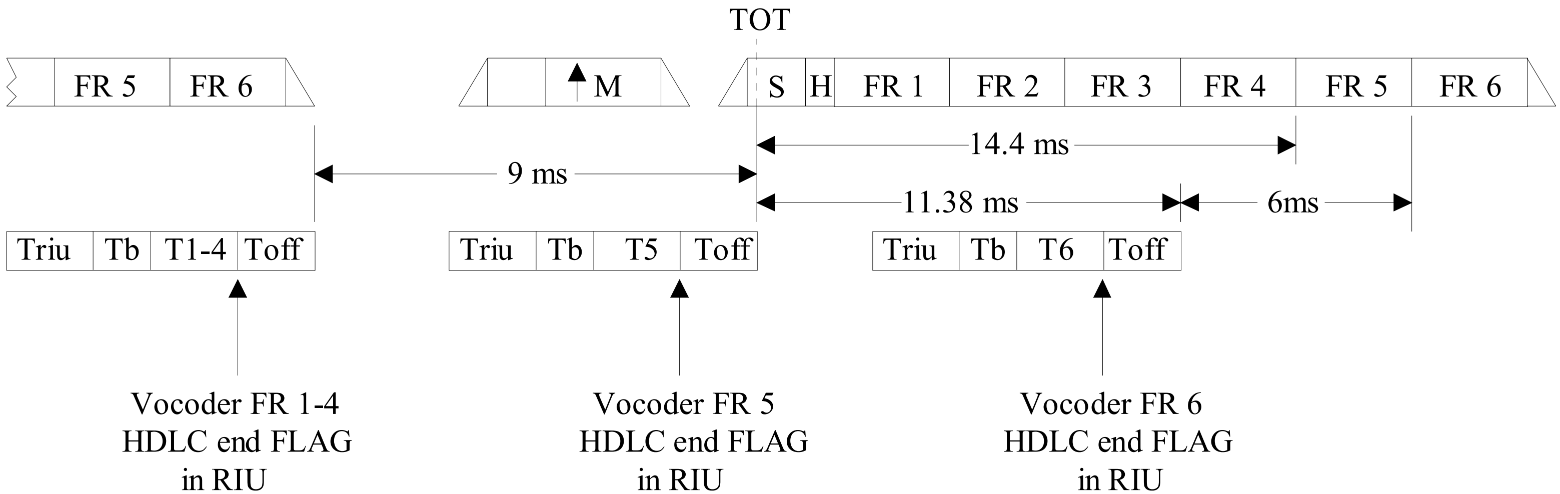
Figure D-4 shows a practical example of uplink Voice-Burst message timing between the RIU and the MDR. The message timing in this example ensures that the Voice-Burst message, which contains vocoder frame 6, arrives at the MDR at least 6 ms prior to when the first D8PSK symbol in vocoder frame 6 is modulated. To further minimize voice delay, vocoder frame 6 is not grouped with any other vocoder frames in the Voice-Burst message. These are “hard” requirements that must be met within the RIU and MDR transmitter.

The MDR transmitter must be capable of continuous modulation of voice in all time slots for all user groups. In 4-slot configurations, the MDR must be capable of processing all Voice-Burst messages associated with a voice time slot, and complete data processing within 30 ms.

In the example shown in Figure D-4, vocoder frames 1-4 are grouped together and arrive at the MDR at a time prior to the end of the ramp-down for the voice burst in the previous time slot (4-slot configuration). This gives the MDR transmitter at least 8.5 ms to process the (24,12) Golay header and the first Voice-Burst message segment prior to the voice burst ramp-up in the upcoming time slot. Vocoder frame 5 is not grouped with any other vocoder frames and it arrives at the MDR no later than the time specified in the Voice-Burst message TOT field. This gives the MDR at least 11.4 ms to process vocoder frame 5 before vocoder frame 6 arrives. The MDR then has at least 6 ms to complete processing of vocoder frame 6.

The timing shown in Figure D-4 is an example that shows one way to implement uplink voice message transmission from the RIU to the MDR transmitter. Other voice frame grouping (for frames 1-5) and message timing is possible and will depend on the processing capabilities in the both the RIU and the MDR transmitter.

The RIU will be required to deliver voice, data and management burst messages to an MDR transmitter over the T1 link far enough in advance to allow sufficient processing time in the MDR prior to ramp-up or continuation of D8PSK modulation. Table D-1 and Figure D-5 show a set of five message timing parameters, T_{M1} - $T_{M5,}$ that will be specified by the MDR manufacturer. The absolute maximum limit for each message timing parameter is also shown in Table D-1. Parameter T_{M1} is the maximum time allocated for the MDR to process the first Voice-Burst message segment (VFSN = 1) and is measured from the arrival of the Voice-Burst message HDLC end flag to the start of voice burst ramp-up. Parameter T_{M2} is the maximum time allocated for the MDR to process a Voice-Burst message that starts with voice segment 2 through 5 and begin modulating the first D8PSK symbol contained in the Voice-Burst message VF field. Parameter T_{M3} is the maximum time allocated for the MDR to process a Voice-Burst message that has the last voice frame (VFSN = 6) and begins modulating the first D8PSK symbol in the Voice-Burst message. Parameter T_{M4} is the maximum time allocated for the MDR to prepare for modulation of a Data Burst after receipt of all 6-segments of the Data Burst message. Parameter T_{M5} is the maximum time allocated for the MDR to prepare for modulation of a Management Burst after receipt of a Management-Burst message.



Parameter	Duration (ms)	Description
Triu	4.0	RIU processing time
Tb	2.2	T1 line blockage
T1-4	2.0	T1 msg TX vocoder frames 1-4
Toff	variable	T1 propagation time RIU-to-MDR
T5	0.84	T1 msg Tx vocoder frame 5
T6	0.84	T1 msg Tx vocoder frame 6

Note: Drawing not to scale

Figure D-4. RIU/MDR Uplink Voice Message Timing

The RIU will coordinate the timing of Voice, Data and Management burst message transmissions to the MDR transmitter such that the HDLC end flag for each message arrives at the MDR within the T_{M1}-T_{M5} parameter limits specified by MDR manufacturer.

Note that the T_{M1}-T_{M5} timing parameters overlap and do not necessarily indicate the amount of time the MDR has to process each message or message segment. If the RIU delivers the Voice, Data or Management burst message on time, the MDR is required to complete HDLC message processing, and initiate or continue D8PSK modulation at the appropriate point in the uplink burst as specified in the message header.

Additional MDR Transmitter requirements are needed to specify what to do when Voice, Data or Management burst messages are incomplete, received in error, or not received in time to be modulated (e.g. if the RIU violates the T_{M1}-T_{M5} timing parameters). In the case of Data, Management, and Voice (with VFSN=1) messages, the data should be discarded and the entire burst should not be modulated. When an MDR has begun modulation of a Voice burst and the Voice-Burst message that contains voice segment 2-6 is not received in time, the MDR should continue voice burst modulation by repeating the data from the last voice frame received from the RIU. In both cases the MDR should set the "V" underflow bit in the next RIU/MDR Status message sent to the RIU.

Table D-1. MDR Transmitter Voice, Data and Management Message Timing Parameters

From receipt of HDLC END flag in RIU message	**To**	**MDR Message Timing Parameter**	**Absolute Maximum (milliseconds)**
Voice-Burst (VFSN=1)	Start of Voice Burst ramp-up	T_{M1}	8.5
Voice-Burst (VFSN=2-5)	Start of modulation of 1st D8PSK symbol in message	T_{M2}	8.5
Voice-Burst (VFSN=6)	Start of modulation of 1st D8PSK symbol in message	T_{M3}	6.0
Data –Burst (containing 6th data segment)	Start of Data Burst ramp-up	T_{M4}	30.0
Management-Burst	Start of Management Burst ramp-up	T_{M5}	90.0

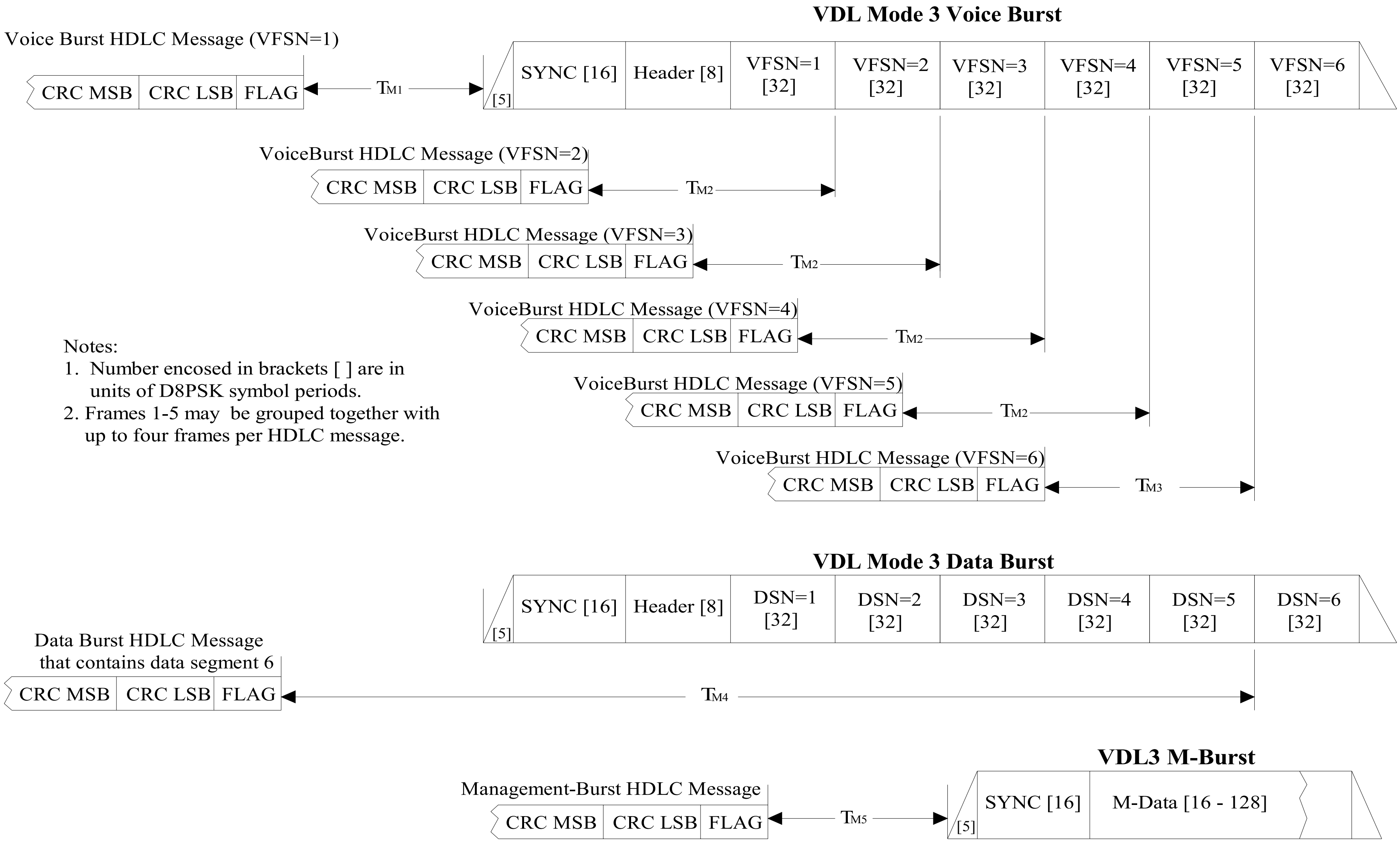


Figure D-5. MDR Transmitter Uplink Burst Timing Parameters (T_{M1}-T_{M3})

APPENDIX E. Message Format Example

An example of Management-Burst message is provided in this appendix to further clarify the message format and is for informational purpose only.

E.1 Management-Burst Message – Uplink (Normal Message)

E.1.1 Header Field Values:

LLMSGID = 2
STYPE = 3 (S_2*)
LEN = 48 = 030h
TOA/TOT = 20160 = 04EC0h
GEC = 0
GEC2 = 0
PWR = 426 = 1Ah

E.1.2 Payload Field Values:

For bit mappings of individual fields within payload octets, refer to the Manual on VHF Digital Link (VDL) Mode 3 Technical Specifications (20 January 2000), Figure B-2, M Uplink (Normal Message).

MESSAGE ID = 0
VOICE SIGNAL = 2
AIRCRAFT ID (POLL) = 6
SYSTEM CONFIGURATION = 3 (2V2D)
SLOT ID = 0
GROUND STATION CODE = 7
SQUELCH WINDOW = 0
RESERVATION RESPONSE #1 = 89 = 059h (User Group A, AC #5 starts in odd 'C' time slot)
RESERVATION RESPONSE #2 = 0

In Figure E-1 below, the msb of each octet (Bit 8) is left. The lsb of each octet (Bit 1) is right. The lsb of each octet (Bit 1) is the first bit transmitted over the T1 data channel.

Octet No.	Octet Value	Bit 8 (msb)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1 (lsb)
1	7Eh	(msb) HDLCFLAGSEQ = 7Eh (lsb)							
2	02h	(msb) HDLCADDR = 02h (lsb)							
3	03h	(msb) HDLCCTRL = 03h (lsb)							
4	02h	(msb) LLMSGID = 2 (lsb)							
5	03h	Spare = 0						(msb) STYPE=3 (lsb)	
6	00h	Spare = 0							
7	03h	(msb) LEN = 03h							
8	00h	(msb) TOA/TOT = 0h				LEN = 0h (lsb)			
9	4Eh	TOA/TOT = 4Eh							
10	C0h	TOA/TOT = C0h (lsb)							
11	00h	Spare=0	(msb) GEC2 = 0 (lsb)			Spare=0	(msb) GEC = 0 (lsb)		
12	1Ah	(msb) PWR = 1Ah (lsb)							
13	08h	MB [0] = 08h							
14	63h	MB [1] = 63h							
15	38h	MB [2] = 38h							
16	05h	MB [3] = 05h							
17	90h	MB [4] = 90h							
18	00h	MB [5] = 00h							
19	E0h	(msb) HDLCFRAMECHK = E0h							
20	5Ch	HDLCFRAMECHK = 5Ch (lsb)							
21	7Eh	HDLCFLAGSEQ = 7Eh							

Figure E-1. Example of Management-Burst Message

APPENDIX F. Verification Requirements Testability Matrix (VRTM).

Table F-1. Verification Requirements Testability Matrix

D=Demonstration I=Inspection A=Analysis T=Test X=Not Applicable						
Section 3 Requirements Paragraph Reference			Verification Method			
			Inspection	Analysis	Test	Demonstration
2	3.2.2.1.4.3.2.15	The bit format of the Software Version parameter **shall** be encoded/decoded as indicated in Figure 3-50.				
4	3.2.2.1.4.3.2.5	The bit format of the MDR State parameter **shall** be encoded/decoded as indicated in Figure 3-40.				
8	3.2.2.1.4.3.2.3	The bit format of the Lowest Tunable Frequency parameter **shall** be encoded/decoded as indicated in Figure 3-38.				
12	3.2.2.1.4.3.2.36	The bit format of the MDR ID Number parameter **shall** be encoded/decoded as indicated in Figure 3-66.				
14	3.2.2.1.4.3.2.20	The bit format of the Transmission Timeout Setting parameter **shall** be encoded/decoded as indicated in Figure 3-55.				
16	3.2.2.1.4.3.2.12	The bit format of the Power Output Setting parameter **shall** be encoded/decoded as indicated in Figure 3-47.				
18	3.2.2.1.4.3.2.13	The bit format of the Transmitter Modulation % Setting parameter **shall** be encoded/decoded as indicated in Figure 3-48.				
20	3.2.2.1.4.3.2.37	The bit format of the RF Input Power Level parameter **shall** be encoded/decoded as indicated in Figure 3-67.				
24	3.2.2.1.4.3.2.21	The bit format of the Squelch Enable/Disable parameter **shall** be encoded/decoded as indicated in Figure 3-56.				
26	3.2.2.1.4.3.2.38	The bit format of the Squelch Break Status parameter **shall** be encoded/decoded as indicated in Figure 3-68.				
28	3.2.2.1.4.3.2.8	The bit format of the Squelch RF Threshold Level Setting parameter **shall** be encoded/decoded as indicated in Figure 3-43.				

D=Demonstration I=Inspection A=Analysis T=Test X=Not Applicable						
Section 3 Requirements Paragraph Reference			Verification Method			
			Inspection	Analysis	Test	Demonstration
32	3.2.2.1.4.3.2.39	The bit format of the In-service Time parameter **shall** be encoded/decoded as indicated in Figure 3-69.				
34	3.2.2.1.4.3.2.4	The bit format of the Mode of Operation parameter **shall** be encoded/decoded as indicated in Figure 3-39.				
36	3.2.2.1.4.3.2.2	The bit format of the Current Frequency parameter **shall** be encoded/decoded as indicated in Figure 3-37.				
38	3.2.2.1.4.3.2.7	The bit format of the Time parameter **shall** be encoded/decoded as indicated in Figure 3-42.				
44	3.2.2.1.4.3.2.11	The bit format of the Receiver Mute parameter **shall** be encoded/decoded as indicated in Figure 3-46.				
48	3.2.2.1.4.3.2.10	The bit format of the Audio Output Level parameter **shall** be encoded/decoded as indicated in Figure 3-45.				
50	3.2.2.1.4.3.2.40	The bit format of the RIU Timing Offset Change parameter **shall** be encoded/decoded as indicated in Figure 3-70.				
54	3.2.2.1.4.3.2.1	The bit format of the Event Log parameter **shall** be encoded/decoded as indicated in Figure 3-36.				
66	3.2.2.1.4.3.2.41	The bit format of the Transmit Antenna VSWR parameter **shall** be encoded/decoded as indicated in Figure 3-71.				
69	3.2.2.1.4.3.2.14	The bit format of the ATR Switch State parameter **shall** be encoded/decoded as indicated in Figure 3-49.				
75	3.2.2.1.4.3.2.16	The bit format of the N1 parameter **shall** be encoded/decoded as indicated in Figure 3-51.				
77	3.2.2.1.4.3.2.17	The bit format of the T1 parameter **shall** be encoded/decoded as indicated in Figure 3-52.				
79	3.2.2.1.4.3.2.18	The bit format of the T3 parameter **shall** be encoded/decoded as indicated in Figure 3-53.				

D=Demonstration I=Inspection A=Analysis T=Test X=Not Applicable						
Section 3 Requirements Paragraph Reference			Verification Method			
			Inspection	Analysis	Test	Demonstration
81	3.2.2.1.4.3.1.1	The bit format of the Log-in/Log-out parameter **shall** be encoded/decoded as indicated in Figure 3-3.				
83	3.2.2.1.4.3.1.2	The bit format of the Current Frequency parameter **shall** be encoded/decoded as indicated in Figure 3-4.				
87	3.2.2.1.4.3.1.3	The bit format of the Lowest Tunable Frequency parameter **shall** be encoded/decoded as indicated in Figure 3-5.				
89	3.2.2.1.4.3.1.4	The bit format of the Mode of Operation parameter **shall** be encoded/decoded as indicated in Figure 3-6.				
91	3.2.2.1.4.3.1.5	The bit format of the MDR State parameter **shall** be encoded/decoded as indicated in Figure 3-7.				
93	3.2.2.1.4.3.1.6	The bit format of the Threshold Setting parameter **shall** be encoded/decoded as indicated in Figure 3-8a.				
95	3.2.2.1.4.3.1.23	The bit format of the Request Read Back parameter **shall** be encoded/decoded as indicated in Figure 3-25a.				
97	3.2.2.1.4.3.1.7	The bit format of the Time parameter **shall** be encoded/decoded as indicated in Figure 3-9.				
99	3.2.2.1.4.3.1.8	The bit format of the Squelch RF Threshold Level Setting parameter **shall** be encoded/decoded as indicated in Figure 3-10.				
103	3.2.2.1.4.3.1.10	The bit format of the Audio Output Level parameter **shall** be encoded/decoded as indicated in Figure 3-12.				
105	3.2.2.1.4.3.1.11	The bit format of the Receiver Mute parameter **shall** be encoded/decoded as indicated in Figure 3-13.				
107	3.2.2.1.4.3.1.12	The bit format of the Power Output parameter **shall** be encoded/decoded as indicated in Figure 3-14.				
109	3.2.2.1.4.3.1.13	The bit format of the Transmitter Modulation % parameter **shall** be encoded/decoded as indicated in Figure 3-15.				

D=Demonstration I=Inspection A=Analysis T=Test X=Not Applicable						
Section 3 Requirements Paragraph Reference			Verification Method			
			Inspection	Analysis	Test	Demonstration
111	3.2.2.1.4.3.1.20	The bit format of the Transmission Timeout parameter **shall** be encoded/decoded as indicated in Figure 3-22.				
113	3.2.2.1.4.3.1.24	The bit format of the Audio Input Level parameter **shall** be encoded/decoded as indicated in Figure 3-26.				
119	3.2.2.1.4.3.1.27	The bit format of the MAC Timing Offset Correction parameter **shall** be encoded/decoded as indicated in Figure 3-27.				
121	3.2.2.1.4.3.1.14	The bit format of the ATR Switch State parameter **shall** be encoded/decoded as indicated in Figure 3-16.				
123	3.2.2.1.4.3.1.28	The bit format of the Suppress Alert/Alarm parameter **shall** be encoded/decoded as indicated in Figure 3-28.				
125	3.2.2.1.4.3.1.29	The bit format of the Reset parameter **shall** be encoded/decoded as indicated in Figure 3-29.				
127	3.2.2.1.4.3.1.30	The bit format of the Software Upload Enable/Disable parameter **shall** be encoded/decoded as indicated in Figure 3-30.				
129	3.2.2.1.4.3.1.15	The bit format of the Switch Software Version parameter **shall** be encoded/decoded as indicated in Figure 3-17.				
131	3.2.2.1.4.3.1.31	The bit format of the Software Upload parameter **shall** be encoded/decoded as indicated in Figure 3-31.				
135	3.2.2.1.4.3.1.16	The bit format of the N1 parameter **shall** be encoded/decoded as indicated in Figure 3-18.				
137	3.2.2.1.4.3.1.17	The bit format of the T1 parameter **shall** be encoded/decoded as indicated in Figure 3-19.				
139	3.2.2.1.4.3.1.18	The bit format of the T3 parameter **shall** be encoded/decoded as indicated in Figure 3-20.				

D=Demonstration I=Inspection A=Analysis T=Test X=Not Applicable						
Section 3 Requirements Paragraph Reference			Verification Method			
			Inspection	Analysis	Test	Demonstration
140	3.2.2.1.4.3.3.1	For the MDR transmitters, the RIU/MDR Status word **shall** comprise the fields specified in Table 3-3.				
141	3.2.2.1.4.3.3.1.1	The S bits indicate the operational status of the MDR component and **shall** be encoded/decoded as follows: 0 = Offline, 1 = Power Down (if exercised), 2 = Power Up, 3 = Online, 4-5 = Reserved, 6 = Recovery, 7= Fail.				
142	3.2.2.1.4.3.3.1.2	The T bit **shall** be encoded as follows: 0 = MDR MAC cycle timing not locked to 6-second epoch, 1 = MDR MAC cycle timing locked to 6-second epoch.				
143	3.2.2.1.4.3.3.1.3	The I bit **shall** be encoded as 1 if any invalid data was received from the RIU during the last MAC cycle, or 0 otherwise.				
144	3.2.2.1.4.3.3.1.4	The F bit **shall** be encoded as 1 if a T1 Frame Slip was detected on the link from the RIU, or 0 otherwise.				
146	3.2.2.1.4.3.3.1.6	The M bit **shall** be encoded as 1 if any M-channel data within the last MAC cycle was not received from the RIU in time to be modulated, or 0 otherwise.				
147	3.2.2.1.4.3.3.1.7	The V bit **shall** be encoded as 1 if any Voice Channel data within the last MAC cycle was not received from the RIU in time to be modulated, or 0 otherwise.				
148	3.2.2.1.4.3.3.1.8	The D bit **shall** be encoded as 1 if any Data Channel data within the last MAC cycle was not received from the RIU in time to be modulated, or 0 otherwise.				
149	3.2.2.1.4.3.3.2	For the MDR receiver, the RIU/MDR Status word **shall** comprise the fields specified in Table 3-4.				

D=Demonstration I=Inspection A=Analysis T=Test X=Not Applicable						
Section 3 Requirements Paragraph Reference			Verification Method			
			Inspection	Analysis	Test	Demonstration
150	3.2.2.1.4.3.3.2.1	The S bits indicate the operational status of the MDR component and **shall** be encoded as follows: 0 = Offline, 1 = Power Down (if exercised), 2 = Power Up, 3 = Online, 4-5 = Reserved, 6 = Recovery, 7 = Fail.				
151	3.2.2.1.4.3.3.2.2	The T bit **shall** be encoded as follows: 0 = MDR MAC cycle timing not locked to 6-second epoch, 1 = MDR MAC cycle timing locked to 6-second epoch.				
152	3.2.2.1.4.3.3.2.3	The I bit **shall** be encoded as 1 if any invalid data was received from the RIU during the last MAC cycle, or 0 otherwise.				
153	3.2.2.1.4.3.3.2.4	The F bit **shall** be encoded as 1 if a T1 Frame Slip was detected on the link from the RIU, or 0 otherwise.				
158	3.2.2.6.1	All non-segmented messages or individual message segments (of a segmented message) sent between the MDR and RIU **shall** be transmitted within one frame.				
159	3.2.2.6.1.1	The Flag (F) Sequence field appears at the beginning and end of all frames and **shall** consist of one 0 bit followed by six contiguous 1 bits and one 0 bit.				
160	3.2.2.6.1.2	For all HDLC messages except the TEST Response message, the AD field **shall** contain the address of the unit **to** which the information sequence in the frame is sent.				
161	3.2.2.6.1.3	The Control (CN) field consists of one octet and **shall** be used to identify the frame type, either TEST or Unnumbered Information (UI).				
162	3.2.2.6.1.4	In a UI frame, the I field **shall** contain a message.				
163	3.2.2.6.1.4	The I field **shall** consist of an integral number of octets.				

D=Demonstration I=Inspection A=Analysis T=Test X=Not Applicable						
Section 3 Requirements Paragraph Reference			Verification Method			
			Inspection	Analysis	Test	Demonstration
164	3.2.2.6.1.5	The Frame Check Sequence (FCS) field **shall** consist of 16 bits and be used for frame error detection.				
165	3.2.2.6.2.1	These two states of operation **shall** be defined as the *link inactive* state and *link initialized* state.				
166	3.2.2.6.2.1	The Link Initialization procedure **shall** consist of the RIU generating a Test Command to the MDR with a four-octet (octet 1 is MSB, octet 4 is LSB) I field consisting of a sequence number starting at zero and incrementing by one with each retransmission.				
168	3.2.2.6.2.3	While in the *link initialized* state, the initiator of the Link Clearing procedure **shall** send a TEST Command message with an five-octet information field, the first four octets (octet 1 is MSB, octet 4 is LSB) containing all ONEs indicating a clear, followed by a one octet clearing cause code.				
169	3.2.2.6.2.3	The recipient of the line clearing procedure **shall** confirm the clear by issuing a TEST Response with the first four octets set to all ONEs.				
171	3.2.2.6.4	The timing and size of HDLC frame transmissions between the MDR and RIU **shall** be controlled such that the voice delay from start of first bit at the originator (MDR/RIU) to the reception of the last bit at the recipient (MDR/RIU), due to HDLC frame transmission, does not exceed 3 ms.				
172	3.2.2.6.5	Each message exchanged across the data interface **shall** contain a one octet Message ID followed by the message.				
176	3.2.2.6.5.1.1	The Voice-Burst message **shall** be encoded as illustrated in Figure 3-77 with the field descriptions shown in Table 3-8.				

D=Demonstration I=Inspection A=Analysis T=Test X=Not Applicable						
Section 3 Requirements Paragraph Reference			Verification Method			
			Inspection	Analysis	Test	Demonstration
178	3.2.2.6.5.1.2	The Data-Burst message **shall** be encoded as illustrated in Figure 3-78 with the field descriptions shown in Table 3-9.				
180	3.2.2.6.5.1.3	The Management-Burst message **shall** be encoded as illustrated in Figure 3-79 with the field descriptions shown in Table 3-10.				
183	3.2.2.6.5.1.3	The Synchronization Header Type (STYPE) field **shall** be encoded per Table 3-10a.				
186	3.2.2.6.5.1.4	The Sync Search Control message **shall** be encoded as illustrated in Figure 3-80 with the field descriptions shown in Table 3-11.				
191	3.2.2.6.5.1.5	The PCM Voice message **shall** be encoded as illustrated in Figure 3-81 with the field descriptions shown in Table 3-12.				
193	3.2.2.6.5.1.6	The Radio Control message **shall** be encoded as illustrated in Figure 3-82 with the field descriptions shown in Table 3-13.				
194	3.2.2.6.5.1.6	The Radio Control message **shall** be segmented across the interface if the message exceeds the segmentation size, defined by the N1 parameter.				
195	3.2.2.6.5.1.6	The Total Segment Count (TSC) field **shall** indicate one less than the total number of segments for a specific transaction (identified by the TID field).				
196	3.2.2.6.5.1.6	The Segment Count (SC) field **shall** indicate the individual segment number for the transaction.				
197	3.2.2.6.5.1.6	A message **shall** be deemed valid by the receiver, if all segments are received in sequence prior to the expiration of the T3 timer.				
200	3.2.2.6.5.1.7	The Radio Monitoring message **shall** be encoded as illustrated in Figure 3-82 with the field descriptions shown in Table 3-13.				

D=Demonstration I=Inspection A=Analysis T=Test X=Not Applicable						
Section 3 Requirements Paragraph Reference			Verification Method			
			Inspection	Analysis	Test	Demonstration
201	3.2.2.6.5.1.7	The Radio Monitoring message **shall** be segmented across the interface if the message exceeds the segmentation parameter, as defined by the parameter N1.				
202	3.2.2.6.5.1.7	The TSC field **shall** indicate one less than the total number of segments for a specific transaction (identified by the TID field).				
203	3.2.2.6.5.1.7	The SC field **shall** indicate the individual segment number for the current transaction.				
204	3.2.2.6.5.1.7	A message **shall** be deemed valid by the receiver, if all segments are received in sequence prior to the expiration of the T3 timer.				
205	3.2.2.6.5.1.7	Monitoring messages generated by the MDR as a result of an Alert or Alarm threshold crossing, **shall** set the RR and TID fields to 0.				
208	3.2.2.6.5.1.8	The RIU/MDR Status message **shall** be encoded as illustrated in Figure 3-83 with the field descriptions shown in Table 3-15.				
209	3.2.2.7	The MDR/RIU interface **shall** implement the fractional T1 protocol as defined in ANSI T1.403-1995.				
210	3.2.2.7.1.1	A T1 frame **shall** consist of 193 bits.				
211	3.2.2.7.1.1	Each T1 frame **shall** be composed of one framing bit and twenty-four 8-bit time slots that carry data.				
212	3.2.2.7.1.1	The framing bit **shall** be the first bit of each frame.				
213	3.2.2.7.1.1	The twenty-four 8-bit slots **shall** be organized as described in Figure 3-82, T1 System Timing.				
214	3.2.2.7.1.1	The T1 line **shall** transmit at a rate of 8,000 T1 frames/s, resulting in a bit rate of 1.544 Mbit/s.				

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215	3.2.2.7.1.1	The T1 line **shall** use Extended Super Frame (ESF) formatting consisting of groups of 24 consecutive T1 frames.				
216	3.2.2.7.1.1	The eighth bit of every time-slot in every sixth T1 frame **shall** be used for data. In other words, robbed bit signaling is not to be used.				
217	3.2.2.7.1.1	The ESF data link **shall** support the Line Loopback Activate/Deactivate and Payload Loopback Activate/Deactivate messages to support line diagnostics and maintenance.				
218	3.2.2.7.1.1	Pulse density **shall** be accomplished using the Bipolar 8-Zero Substitution (B8ZS) method.				
219	3.2.2.7.1.2	Each T1 port **shall** be able to operate over any cable length between 0 and 6,000 ft.				
220	3.2.2.7.1.2	Each T1 port **shall** incorporate transient protection.				
221	3.2.2.7.1.2	Each T1 port **shall** have a jitter tolerance that conforms to [ITU-T Recommendation G.824 (03/93), Section 3.1.1, Table 2].				
222	3.2.2.7.1.3	These slots **shall** be allocated according to the following subparagraph.				
223	3.2.2.7.1.3.1.a	Time slots one and two **shall** be used to carry information in a timing channel.				
224	3.2.2.7.1.3.1.b	Time slots three and four **shall** be unused, and designated as spares.				
225	3.2.2.7.1.3.1.c	The remaining time slots (5 through 24) in the T1 frame **shall** be organized into five data channels, each consisting of four contiguous T1 time slots.				
226	3.2.2.7.1.3.1.d	The default data channel **shall** be channel 1 (slots 5 - 8).				
227	3.2.2.7.1.3.2.a	Timing **shall** be conveyed in the timing channel using a 16-bit counter that increments by one for each T1 frame.				

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228	3.2.2.7.1.3.2.b	The first timing slot **shall** contain the low-order least significant byte (LSB) of the counter with the most significant bit of the byte transmitted/received first.				
229	3.2.2.7.1.3.2.c	The second timing slot **shall** contain the high-order most significant byte (MSB) of the counter with the most significant bit of the byte transmitted/received first.				
230	3.2.2.7.1.3.2.d	Bit 1 (least significant bit) of each HDLC message octet **shall** be the first bit transmitted over the Data Channel on the T1 line.				
237	3.2.2.7.1.3.3.b	Each data channel **shall** be capable of carrying data, control, monitoring and status information in the VDL Mode 3 and PCM Voice, control, monitoring and status information in the DSB-AM Mode.				
238	3.2.2.7.1.3.3.c	Allocation of time slots to channels **shall** be fixed for all T1 frames on a given link (i.e., for as long as a channel is in use, it occupies the same time slot numbers in each T1 frame that is generated).				
244	3.2.2.7.2	The leading edge of the framing bit **shall** be the point-of-reference for system timing.				
245	3.2.2.7.2	The leading edge of a framing bit of T1 frame **shall** coincide with the beginning of the VDL Mode 3 6-second epoch within plus or minus 10 microseconds.				

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246	3.2.2.7.2	The start of the 6-second epoch **shall** coincide with the center of the first D8PSK synchronization symbol in LBAC 1 of slot A in the even TDMA frame of the first MAC cycle in the epoch, which is also –1260 D8PSK symbol periods relative to the MAC cycle "0" Timing Reference Point (TRP) as defined in the VDL Mode 3 RTCA DO-224a.				
247	3.2.2.7.2	For Voice-Burst, Data-Burst and Management-Burst Messages, the TOT and TOA fields **shall** have a "0" reference point that corresponds to the center of the first D8PSK synchronization symbol in LBAC 1 of slot A in the even TDMA frame of the MAC cycle in which the burst is transmitted or received.				
251	3.2.2.1.4.3.1.19	The bit format of the HDLC Channel Number Parameter **shall** be encoded/decoded as indicated in Figure 3-21.				
252	3.2.2.1.4.3.1.21	The bit format of the Squelch Enable/Disable parameter **shall** be encoded/decoded as indicated in Figure 3-23.				
253	3.2.2.1.4.3.1.32	The bit format of the Receiver Mute Level parameter **shall** be encoded/decoded as indicated in Figure 3-32.				
254	3.2.2.1.4.3.1.33	The bit format of the Test PTT parameter **shall** be encoded/decoded as indicated in Figure 3-33.				
255	3.2.2.1.4.3.2.6	The bit format of the Threshold Setting parameter **shall** be encoded/decoded as indicated in Figure 3-41.				
256	3.2.2.1.4.3.2.19	The bit format of the HDLC Channel Number Parameter **shall** be encoded/decoded as indicated in Figure 3-54.				

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257	3.2.2.6.2.3	Upon receipt of a valid TEST Response confirming the clear, the initiator **shall** clear the T1 timer, and both the MDR and RIU will be in the *link inactive* state.				
258	3.2.2.6.5.1	Unless otherwise specified in the remainder of this section, bit fields **shall** be encoded such that the most significant bit of a field (or sub-field that crosses octet boundaries) is in the highest bit number position of the octet.				
259	3.2.2.6.5.1	For variable length bit fields that have a total length (LEN) that is not a multiple of 8, the most significant bit of the part-octet (remaining part of the field) at the end of the field **shall**[259] be encoded in bit 8 of the last octet and the unused lower numbered bit(s) in the last octet **shall**[260] be set to 0.				
260	3.2.2.6.5.1	For variable length bit fields that have a total length (LEN) that is not a multiple of 8, the most significant bit of the part-octet (remaining part of the field) at the end of the field **shall**[259] be encoded in bit 8 of the last octet and the unused lower numbered bit(s) in the last octet **shall**[260] be set to 0.				
261	3.2.2.6.5.1.1	The TOA/TOT field **shall** be the same value for all Voice-Burst message segments related to the same VDL Mode 3 voice burst.				
262	3.2.2.6.5.1.1	VDL Mode 3 Voice burst D8PSK symbols **shall** be mapped to Voice-Burst message VF octets as specified in Table 3-8a.				
263	3.2.2.6.5.1.2	The TOA/TOT field **shall** be the same value for all Data-Burst message segments related to the same VDL Mode 3 data burst.				

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264	3.2.2.6.5.1.2	VDL Mode 3 data burst D8PSK symbols **shall** be mapped to Data-Burst message DF octets as specified in Table 3-8a.				
265	3.2.2.6.5.1.3	The MB field **shall** be encoded with the most significant bit of each VDL Mode 3 12-bit Management Burst word placed in the highest unused bit number position in the octet.				
266	3.2.2.6.5.1.3	As Management Burst words cross octet boundaries, the most significant bit of the remaining 12-bit Management Burst word **shall** be placed in bit 8 of the next octet.				
267	3.2.2.6.5.1.4	The Synchronization Header Type (STYPE) field **shall** be encoded per Table 3-10a.				
268	3.2.2.6.5.1.4	The NGW field **shall** indicate the number of (24,12) Golay words in the received burst to be decoded by the MDR if synchronization is achieved within the search window.				
269	3.2.2.7.2	For the Sync Search Control Message, the Sync Search Start (S_START) field **shall** define the earliest time within a VDL Mode 3 epoch where the center of the first D8PSK synchronization symbol in a receive burst may occur.				
270	3.2.2.7.2	For the Sync Search Control Message, the Sync Search Stop (S_STOP) field **shall** define the latest time within a VDL Mode 3 epoch where the center of the first D8PSK synchronization symbol in a receive burst may occur.				
271	3.2.2.7.2	The resolution of the TOA, TOT, S_START and S_STOP fields **shall**[293] be 1/16th of a D8PSK symbol period and **shall**[271] have a range of 0 to 1, 007,999 within a 6-second VDL Mode 3 epoch.				

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272	3.2.2.1.4.3.1.9	The bit format of the Squelch Audio Signal-to-Noise Level Setting parameter **shall** be encoded/decoded as indicated in Figure 3-11.				
273	3.2.2.1.4.3.1.34	The bit format of the Public Key Maintenance parameter **shall** be encoded/decoded as indicated in Figure 3-34.				
274	3.2.2.1.4.3.1.35	The bit format of the T2 parameter **shall** be encoded/decoded as indicated in Figure 3-35.				
275	3.2.2.1.4.3.2.9	The bit format of the Squelch Audio Signal-to-Noise Level Setting parameter **shall** be encoded/decoded as indicated in Figure 3-44.				
276	3.2.2.1.4.3.2.24	The bit format of the Audio Input Level Setting parameter **shall** be encoded/decoded as indicated in Figure 3-58.				
277	3.2.2.1.4.3.2.27	The bit format of the MAC Timing Offset Correction parameter **shall** be encoded/decoded as indicated in Figure 3-59.				
278	3.2.2.1.4.3.2.28	The bit format of the Suppress Alert/Alarm Setting parameter **shall** be encoded/decoded as indicated in Figure 3-60.				
279	3.2.2.1.4.3.2.30	The bit format of the Software Upload Setting parameter **shall** be encoded/decoded as indicated in Figure 3-61.				
280	3.2.2.1.4.3.2.32	The bit format of the Receiver Mute Level Setting parameter **shall** be encoded/decoded as indicated in Figure 3-62.				
281	3.2.2.1.4.3.2.33	The bit format of the PTT Setting parameter **shall** be encoded/decoded as indicated in Figure 3-63.				
282	3.2.2.1.4.3.2.34	The bit format of the Public Key List parameter **shall** be encoded/decoded as indicated in Figure 3-64.				
283	3.2.2.1.4.3.2.35	The bit format of the T2 parameter **shall** be encoded/decoded as indicated in Figure 3-65.				

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284	3.2.2.1.4.3.2.4 3	The bit format of the Measured Power Output parameter **shall** be encoded/decoded as indicated in Figure 3-72.				
285	3.2.2.1.4.3.2.4 4	The bit format of the Measured Transmitter Modulation % parameter **shall** be encoded/decoded as indicated in Figure 3-73.				
286	3.2.2.6.1.2	For TEST Response messages, the AD field **shall** contain the address of the unit **from** which the information sequence in the frame is sent.				
287	3.2.2.6.1.2.1	The MDR **shall** encode the HDLC address as 01 for all HDLC UI messages to be delivered to the RIU.				
290	3.2.2.6.1.3	All Unnumbered Information (UI) frames **shall** be UI Command frames.				
291	3.2.2.6.1.3	The Poll/Final bit (bit 5) in the Control Field is not used and **shall** be set to 0.				
292	3.2.2.6.5.1.6	If the MDR detects an error, it **shall** be reported back in the reply by setting the ER field to 1, and placing the error cause code in the first octet of the message (MSG) field.				
293	3.2.2.7.2	The resolution of the TOA, TOT, S_START and S_STOP fields **shall**[293] be 1/16th of a D8PSK symbol period and **shall**[271] have a range of 0 to 1, 007,999 within a 6-second VDL Mode 3 epoch.				
294	3.2.2.1.4.3.1.2 2	The bit format of the ATR Switch Mode parameter **shall** be encoded/decoded as indicated in Figure 3-24.				
295	3.2.2.1.4.3.2.2 2	The bit format of the ATR Switch Mode parameter **shall** be encoded/decoded as indicated in Figure 3-57.				
296	3.2.2.6.1.2.2.a)	MDR transmitters **shall** encode the HDLC address as 02 for all HDLC Test Response messages to be delivered to the RIU.				

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297	3.2.2.6.1.2.2.b)	MDR receivers **shall** encode the HDLC address as 03 for all HDLC Test Response messages to be delivered to the RIU.				
298	3.2.2.6.1.2.2.d)	MDR transmitters **shall** accept and process HDLC UI messages from the RIU with the HDLC address encoded as 02.				
299	3.2.2.6.1.2.2.e)	MDR receivers **shall** accept and process HDLC UI messages from the RIU with HDLC address encoded as 03.				
300	3.2.2.6.1.6	The time between frames **shall** be filled with flag characters, per ISO 3309.				